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SIERRA

914B DATA TEST SET

DESCRIPTION AND OPERATION

CONTENTS PAGE

1. GENERAL

1.01 This section provides a physical and functional description and operating theory necessary for effective use of the 914B Data Test Set.

1.02 This section is reissued:

(a) To update front panel stampings

(b) To change the titles of Fig. 3, 14 and 15

(c) To revise tests under 6.06 through 6.10, 6.14 and 6.15.

1.03 The 914B Data Test Set is a portable unit which facilitates dynamic and static tests of voiceband data sets. It is used for testing digital and analog data systems. It provides all the functions of the 901, 902, 903, and 913 series of data test sets and introduces several additional features not previously available. A high degree of flexibility is incorporated in the 914B which allows for accommodation of testing requirements of future data systems. Features of the 914B include the following:

Flexibility in establishing all required interface connections

Three types of test messages; dot signal, 63-bit, and 511-bit words are available

Automatic and manual word synchronization

Variable width window for sampling received data

Bit and block error counting

Time-interval measurement

High-impedance ac voltmeter and loudspeaker amplifier to permit line signal monitoring

DC voltmeter

Tests of data services which operate in the range of 10 to 20,000 bits per second

1.04 The 914B Data Test Set may be used at both transmitting and receiving stations of a data system. For an end-to-end test, one 914B is required at the transmitting data station and one at the receiving data station. The 914B may be used at either the transmit or receive station with 901, 902, 903, or 913-type data test sets at the opposite station; however, this reduces the test capability of the 914B.

1.05 The 914B contains a programmable crosspoint matrix which provides the ability to connect the 914B test circuits to the interface leads of a data set. By the application of control signals to the appropriate interface leads, the data set being tested is conditioned to go into the desired operating mode. The control signals from the data set are monitored by lamps in the 914B to determine whether the desired mode of operation has been achieved. Then, depending on the type of data system being tested, test messages are transmitted or received, and the performance characteristics of the data set or data system are checked.

1.06 The program matrix of the 914B provides 25 vertical buses and 24 horizontal buses. The 25 vertical buses connect to the interface connector of the data set being tested; the 24 horizontal buses connect to the test circuits provided by the 914B. Connections from the input or output leads of the test circuits to the interface leads are made by inserting programming pins at the intersections of the appropriate vertical and horizontal buses of the matrix.

1.07 The 914B generates three different digital test messages for testing serial and certain parallel data services:

(a) A 63-bit test word that is compatible with that produced by the 903 series data test sets

(b) A 511-bit test word that conforms to the CCITT (Consultative Committee for International Telephone and Telegraph) standard

(c) A dot signal, ie, alternate marks and spaces.

1.08 Test messages are generated at bit rates determined either by the data set clock or by the internal clock of the 914B. When driven by external clock signals (normally from the data set), the bit rate must be in the range of from 10 bits per second (bps) to 20,000 bps. When testing 402-type data sets, the 914B will generate the test messages at a rate of 75 bps. For tests of serial data sets, the 914B internal clock will produce test messages at bit rates of 150, 300, 600, 1000, 1200, 1400, 1600, 1800, 2000, and 2400 bps.

1.09 When testing serial asynchronous data sets in the receive mode, a bit synchronization signal is recovered from the received data at any of the ten bit rates listed in 1.08. This is accomplished by phase-locking the 914B clock oscillator to the transitions in the received data information. Synchronous data sets that recover their own clock signals may be tested at any bit rate in the range of from 10 to 20,000 bps as determined by the data set characteristics.

1.10 In the receive mode, the test message is synchronized with the received data from the data set and a bit-by-bit comparison is made. Any errors detected are recorded and displayed by a 2-digit electronic counter. A lamp gives an indication when the counting capacity of the counter has been exceeded.

1.11 Word synchronization and error comparison may be accomplished either manually or automatically. In the manual mode, when the WORD SYNC switch is momentarily activated, the recorded error count will represent the true number of errors. In the automatic mode, the count recorded will equal approximately three times the true error count.

1.12 A comparator is provided to sample each received bit with a 0.5 μsec pulse centered at the midbit position. In addition, when testing asynchronous data sets, the width of the sampling pulses may be adjusted in 10-percent steps from 10 to 50 percent of the bit interval. Any discrepancy between the received bit and the corresponding locally generated bit during the sampling interval is registered as an error, thereby providing a means of assessing the error margin.

1.13 When testing 402-type data systems, combinations of three types of test signals (steady space, dot, and either the 63- or 511-bit word) are applied to the eight parallel data channels in the form of contact closures. In the receive mode, the data channels may be tested either individually or simultaneously. In either case, the comparator circuit checks each bit or each parallel group of bits for errors, and records the total number of errors on the counter. One useful mode of operation consists of applying the test message on one channel and dotting signals on the other channels to check for interaction between channels.

1.14 In addition to measuring the average error rate of a data system, the 914B allows block error rates to be determined. In this mode, one or more bit errors in a block of preselected length are registered on the counter as a single count. The block length is selected in certain multiples of the test word length, ie, 63 or 511, and ranges from 63- to 8176-bit intervals.

1.15 The 914B provides two detector circuits which give visual indication of two trouble conditions that may be misleading during testing: (a) the absence of a data output signal during tests of serial data systems and (b) the absence of a clock signal from the data set.

1.16 Analog data sets may be tested by the 914B by applying precise dc voltages to the transmitter data leads and by measuring the receiver data output voltage. The voltages may be selected by a switch in steps or they may be obtained in

a continuously adjustable mode from a high-resolution potentiometer circuit.

1.17 The 914B Data Test Set contains a dc volt-ohm-meter and a high impedance ac voltmeter capable of measuring line signals in the range from −50 to +2 dBm. A loudspeaker-amplifier circuit is also provided to permit audible monitoring of line signals for use in "hands free" operation.

1.18 Eight indicator lamps are provided to monitor control signals to and from the data set. Control signals may be applied by toggle switches to control leads of the data set. Both the indicator lamps and the control switches are compatible with voltage and contact interfaces.

1.19 An interval counter is incorporated in the 914B to indicate visually which of two input signals changes state first and to measure the time interval between the state transitions. The circuit is triggered by voltage transitions of either polarity or by contact closure or openings. In this manner an accurate measurement of elapsed time between two events occurring in the interface may be made.

1.20 Two 25-pin data interface connectors (A and B) are provided and are connected through a bank of push-pull switches (A and B selector switches) to the vertical buses of the program matrix. These selector switches permit tests of a data set on an in-service basis in either a bridging or terminating mode. In addition, they offer means of using the test set with data sets having more than 25 interface leads.

1.21 The voltage interface outputs from the test set are at levels close to the minimum EIA specifications for data sets. Similarly, series and shunt resistors incorporated in contact interface leads simulate the effects of cables used in the normal installation of data systems. These marginal test signals make the data set tests more stringent.

1.22 An attenuator is provided with the 914B and can be connected in shunt with the telephone line at the transmitting end. As a result, the transmit level and thus the signal-to-noise ratio is reduced, thereby increasing confidence in the observed error performance.

2. PHYSICAL DESCRIPTION

2.01 The 914B Data Test Set shown in Fig. 1 and 2 is an integrated unit incorporating all instrumentation necessary to test both statically and dynamically most data services. The cover provides protection of the front panel of the test set and also serves as storage space for two interface connection cables, two test leads, and the 4-dB attenuator pad (see Fig. 3). The test set with its cover in place measures approximately 18-1/2 inches wide, 15 inches high, 7-1/2 inches deep, and weighs about 27 pounds.

2.02 The 914B is powered by a self-contained power supply which draws about 60 watts of 105- to 125-volt 50- to 65-Hz commercial power.

2.03 The 914B is designed to operate efficiently in an environment with an ambient temperature range of +40° to +120°F and a relative humidity of 20 to 95 percent.

Fig. 1—914B Data Test Set—Cover in Place

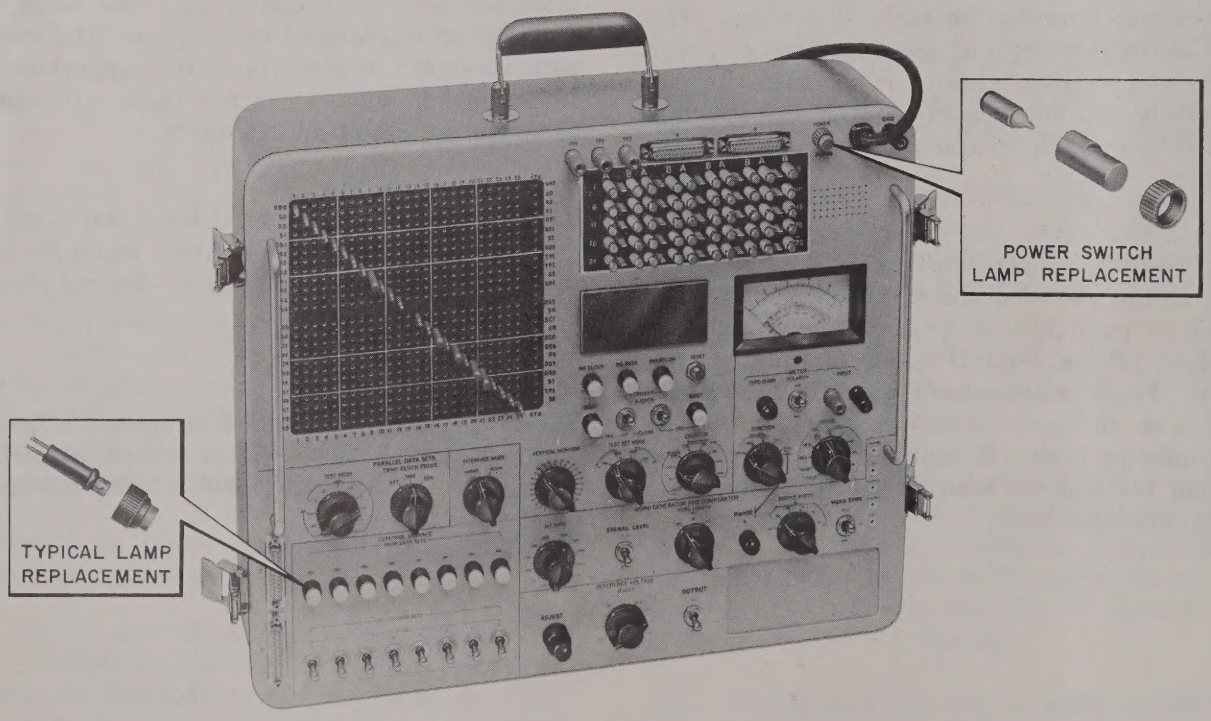

Fig. 2—914B Data Test Set—Front Panel

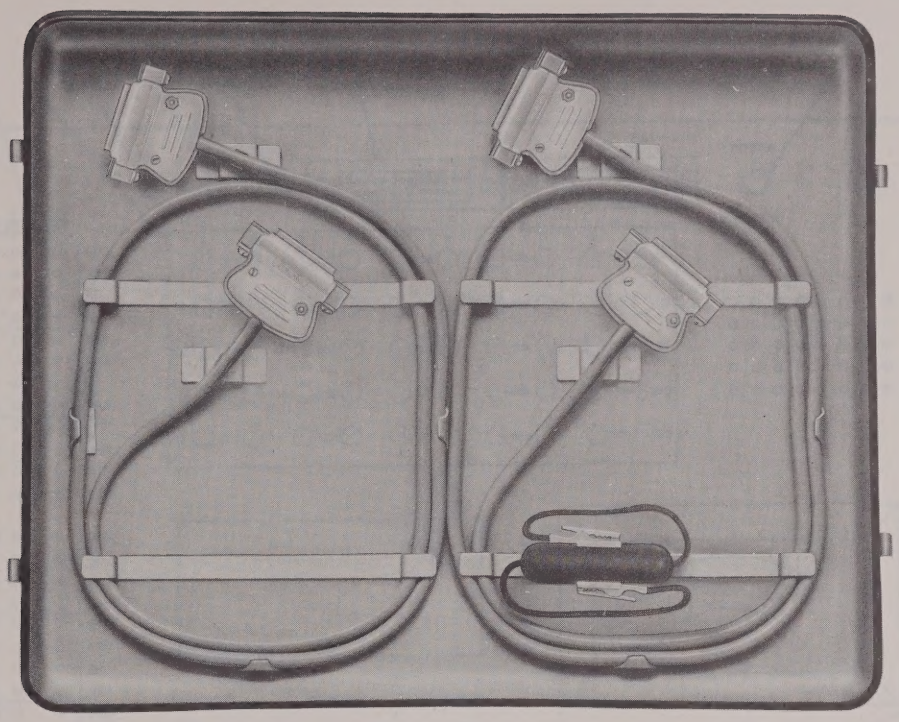

Fig. 3—914B Data Test Set ▶Cover—Cables and Attenuator Pad in Place◀

2.04 Figures 4, 5, and 6 provide number key callouts of all components located on the front panel. Associated Tables A, B and C provide a cross-reference for each callout, identifying the respective part as to function, description, and/or designation.

2.05 The functional designations for the program matrix and switches are abbreviated and stamped on the front of the matrix panel. These designations and their meanings are listed below:

Program Matrix

Designation	Meaning
GRD	Ground
SD	Send data output
RD	Receive data input
SCT	Serial clock transmit input
SCR	Serial clock receive input
DS1-DS8	Inputs to lamps DS1-DS8
S1-S8	Outputs from S1-S8
TP1-TP3	Test point connections
STG	Program pin storage

Switches

CHAN	Parallel data channel
ALL RDM	Random test signal on all channels
ALL SPC	Spacing signal on all channels
ALL DOT	Dot signal on all channels
SER	Serial
WL, 2WL, etc	Word length; block length in multiples of the word length, ie, 63 or 511, selected
AUTO	Automatic
MAN	Manual

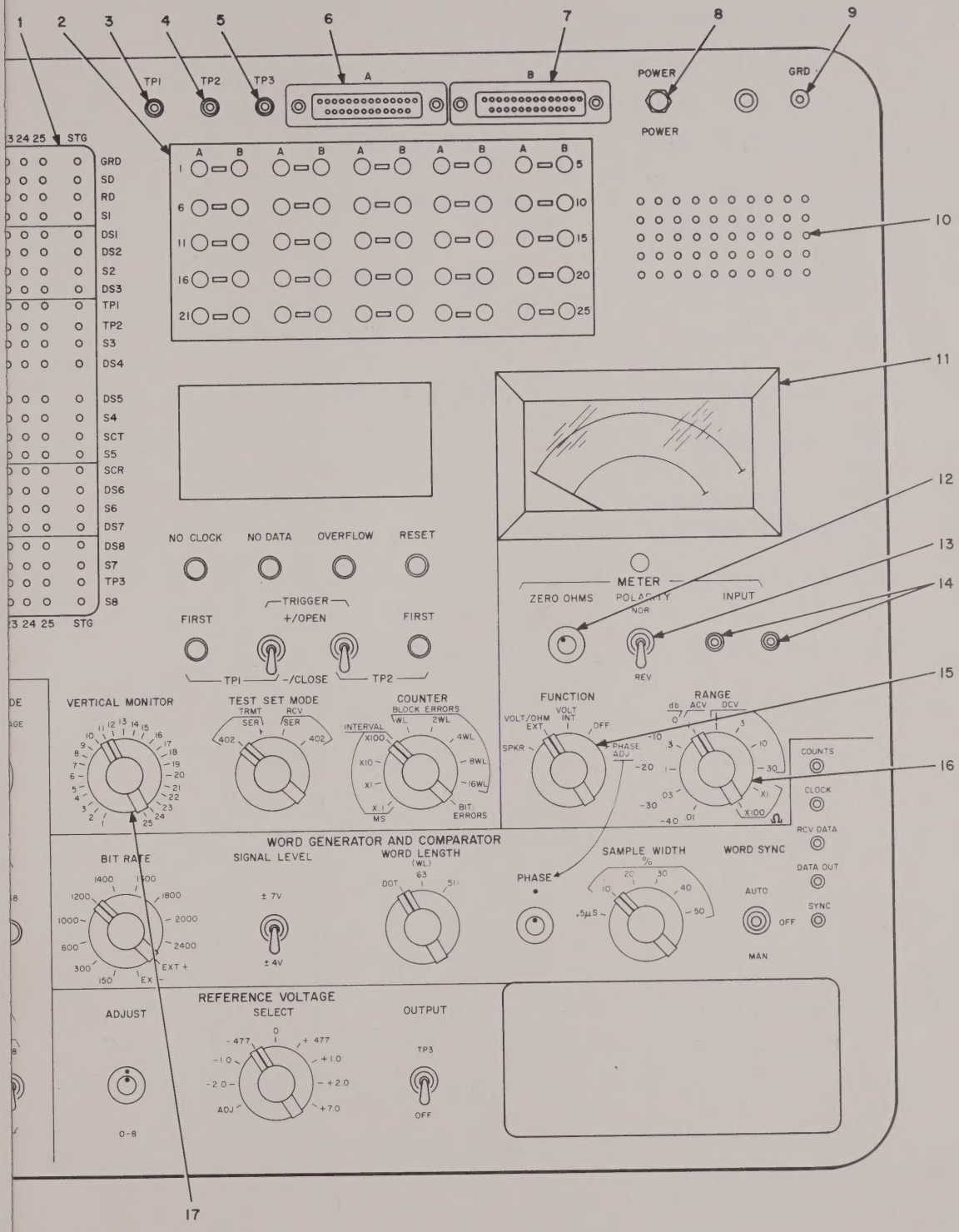

Fig. 4—914B Data Test Set—Controls and Indicators (A)

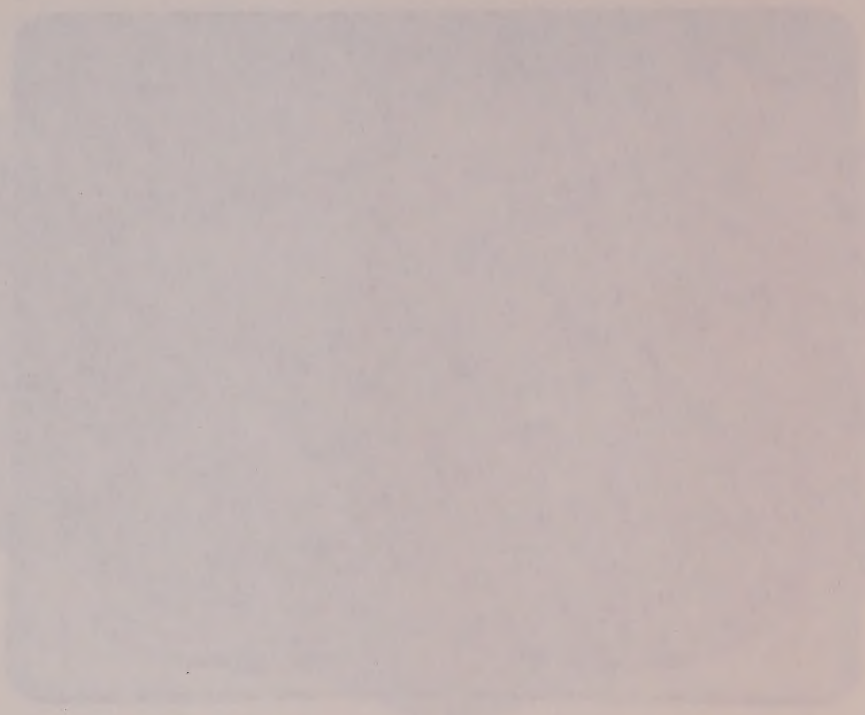

TABLE A

CONTROLS AND INDICATORS

KEY	CONTROL	FUNCTION
1	Program Matrix	Provides access to interface leads of data set being tested.
2	Interface Selector Switches	Provide access to program matrix for in-service testing of data sets.
3	TP1 Test Point	Provides access to interval counter and matrix.
4	TP2 Test Point	Provides access to interval counter and matrix.
5	TP3 Test Point	Provides access to reference voltages and matrix.
6	A Connector	Connected to serial-type data set interface during tests.
7	B Connector	Connected to business machine interface during in-service tests of serial-type data sets.
8	POWER Switch and Lamp	Turns test set on and off and provides power on indication.
9	GRD Terminal	Provides external ground for test set.
10	Loudspeaker	Provides audible monitor of signals on telephone line.
11	Meter	Provides visual indication of ac and dc voltage and resistance.
12	ZERO OHMS Adjustment	Provides ohmmeter calibration for 0 ohms.
13	POLARITY Switch	Facilitates reversal of dc meter polarity.
14	INPUT Terminals	Allow input to speaker and meter from an external circuit. Black terminal is negative and red terminal is positive with respect to the meter when POLARITY switch is in NOR position.
15	FUNCTION Switch	Controls the mode for meter circuit.
16	RANGE Switch	Selects desired meter range for signal measurements. Controls loudspeaker volume when FUNCTION switch is set to SPKR position.
17	VERTICAL MONITOR Switch	Facilitates dc-voltage measurements on any of the interface leads.

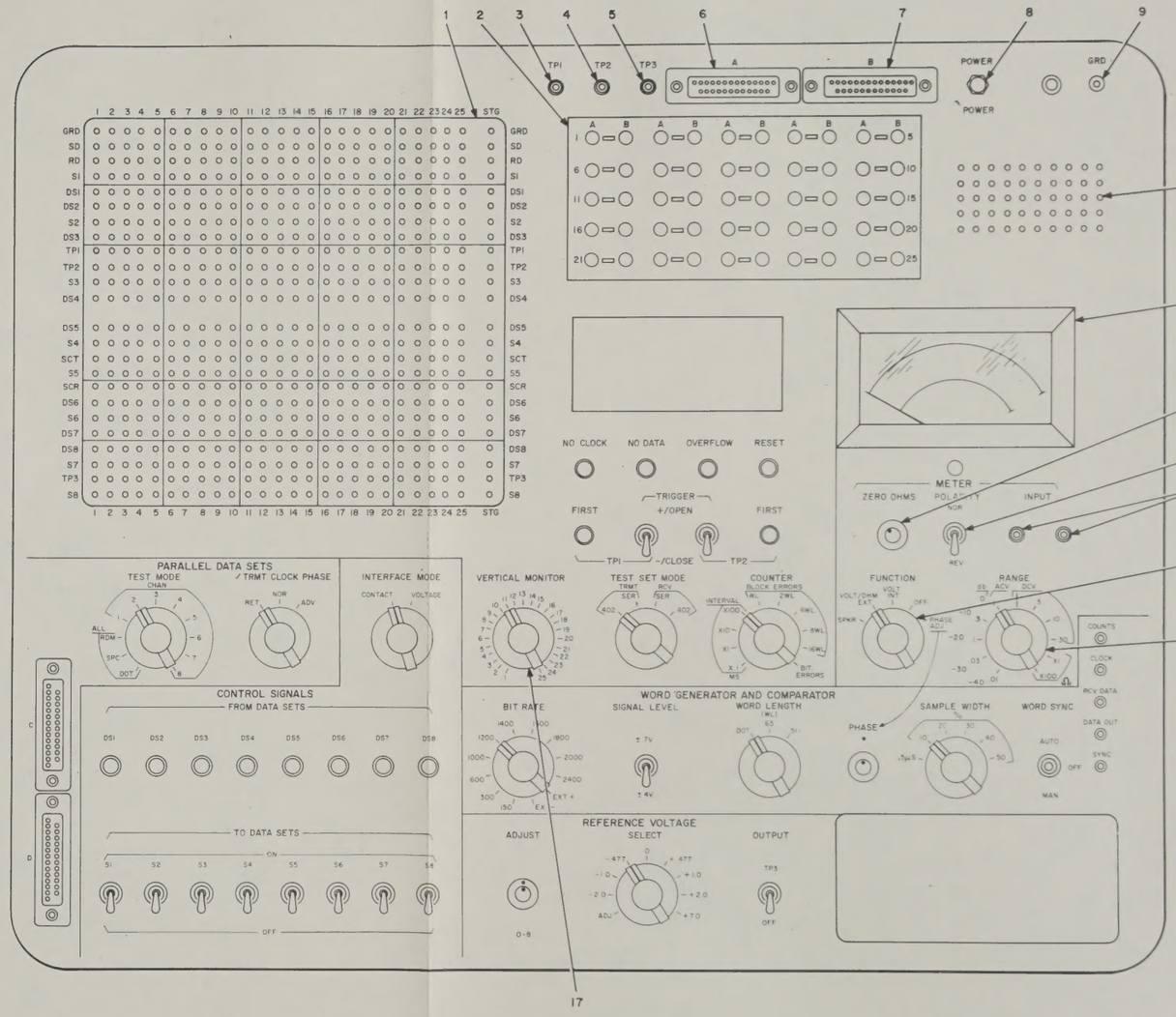

Fig. 4—914B Data Test Set—Controls and Indicators (A)

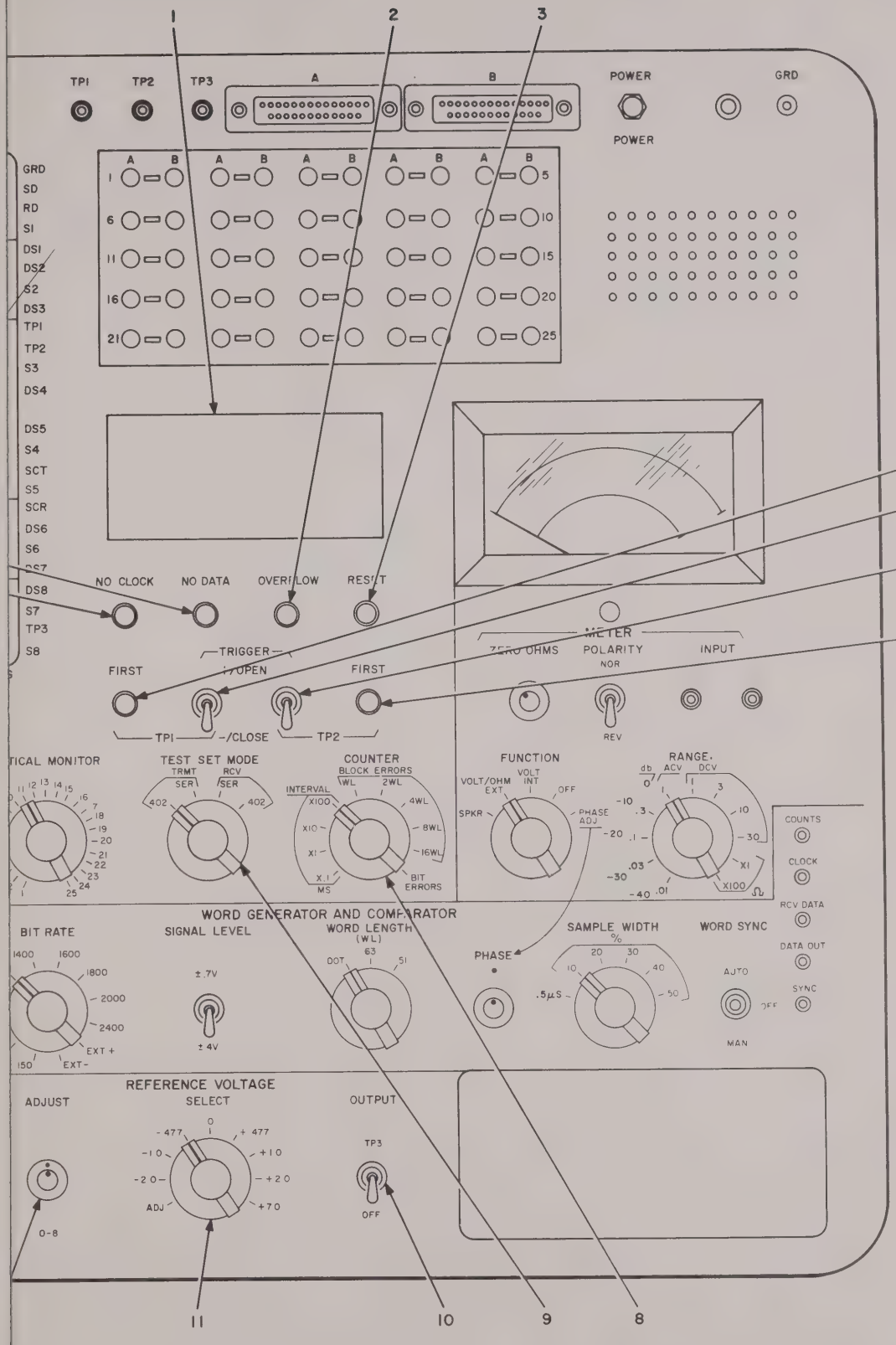

Fig. 5—914B Data Test Set—Controls and Indicators (B)

TABLE B

CONTROLS AND INDICATORS

KEY	CONTROL	FUNCTION
1	Counter Display	Provides decade counter readout from 0 to 99.
2	OVERFLOW Lamp	Lit when counter capacity has been exceeded.
3	RESET Switch	Clears error and interval counter circuits.
4	FIRST TP1 Lamp	Lit when preselected signal appears first on TP1 lead.
5	TP1 TRIGGER Switch	Selects triggering mode on TP1.
6	TP2 TRIGGER Switch	Selects triggering mode on TP2.
7	FIRST TP2 Lamp	Lit when preselected signal appears first on TP2 lead.
8	COUNTER Switch	Provides for either block or bit error rate or interval count.
9	TEST SET MODE Switch	Selects the required test mode (transmit, receive, serial, or parallel) for a particular data set.
10	OUTPUT Switch	Applies selected reference voltage to TP3 and the TP3 horizontal of the matrix.
11	SELECT Switch	Provides for selection of a desired fixed reference voltage.
12	ADJUST Control	Provides coarse and vernier adjustment of a variable reference voltage.
13	NO CLOCK Lamp	Lit during absence of clock signal.
14	NO DATA Lamp	Lit during absence of data signal from data set.

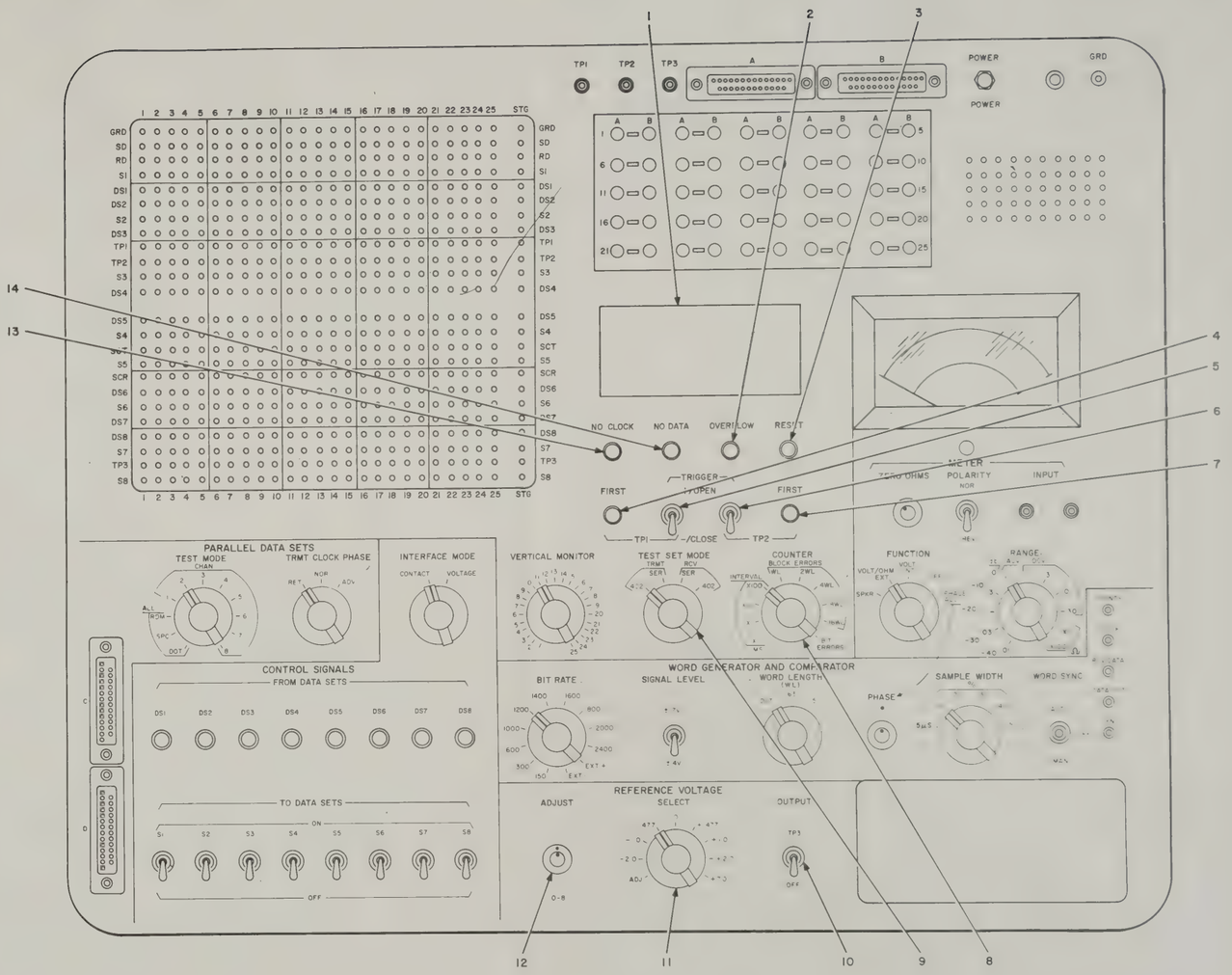

Fig. 5—914B Data Test Set—Controls and Indicators (B)

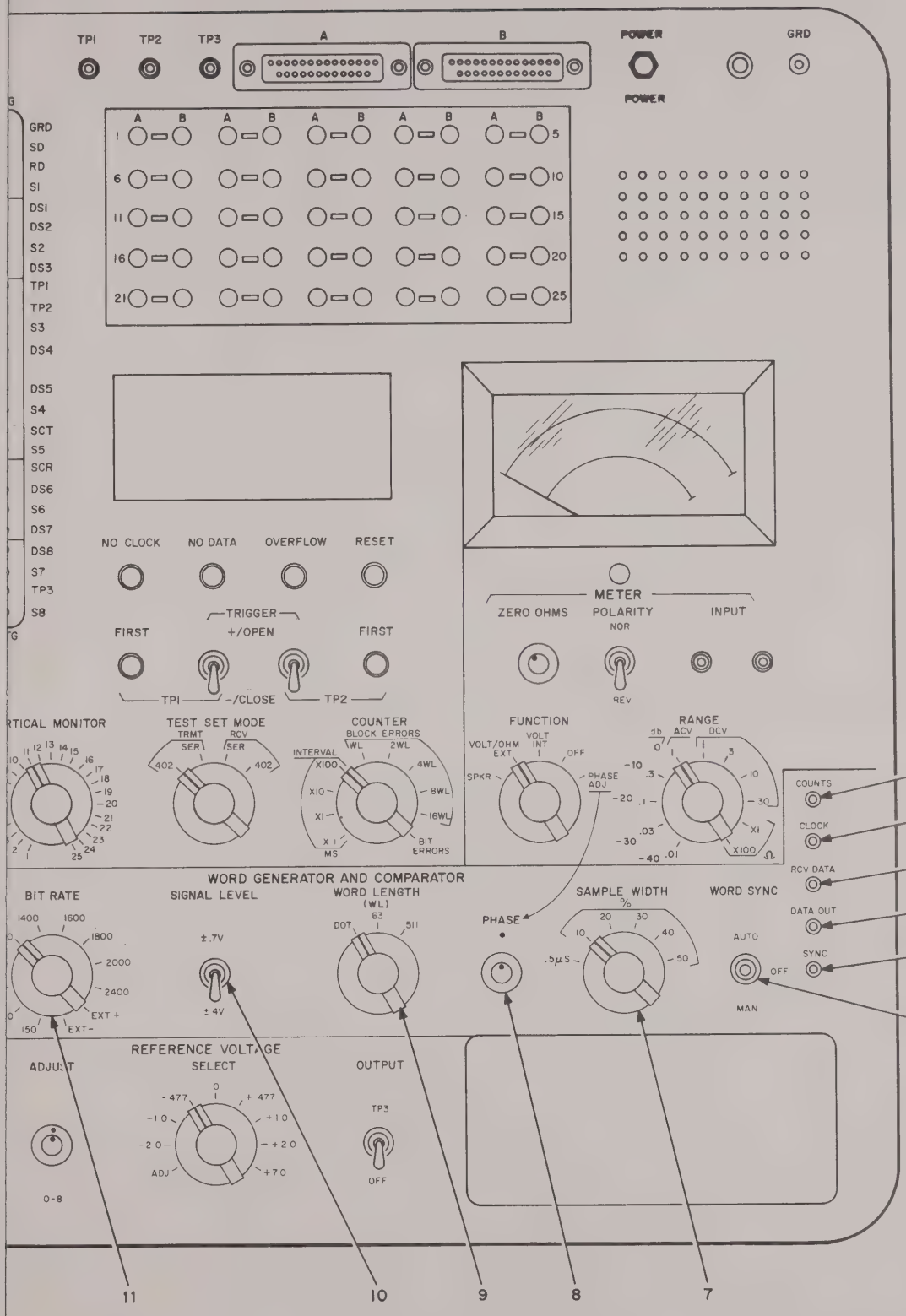

Fig. 6—914B Data Test Set—Controls and Indicators (C)

TABLE C

CONTROLS AND INDICATORS

KEY	CONTROL	FUNCTION
1	COUNTS Test Point	Provides access to a pulse produced for every 100 errors recorded on the external counter.
2	CLOCK Test Point	Provides access to a symmetrical square wave, +4.5 volts in amplitude and equal in frequency to the test set bit rate.
3	RCV DATA Test Point	Provides access to the data signal applied to the RD horizontal row of the program matrix when the test set is in serial receive mode.
4	DATA OUT Test Point	Provides access to the bi-polar data signal produced by the word generator.
5	SYNC Test Point	Provides access to the positive word sync signal, one bit interval in length, occurring once per word.
6	WORD SYNC Switch	Provides for selecting either manual or automatic word synchronization.
7	SAMPLE WIDTH Switch	Provides for selection of sample pulse width.
8	PHASE Adjustment	Provides a fine adjustment of the voltage-controlled oscillator.
9	WORD LENGTH Switch	Provides selection of dot, 63-bit or 511-bit test word.
10	SIGNAL LEVEL Switch	Allows selection of either ±0.7 or ±4 volts for word generator (SD) output level.
11	BIT RATE Switch	Determines rate of timing signal used to drive word generator and comparator.
12	INTERFACE MODE	Selects contact or voltage mode for control signals.
13	DS1-DS8 Lamps	Indicate presence of control signals on eight of the matrix horizontal buses.
14	S1-S8 Switches	Provide control signals.
15	D Connector	Connected to data set during testing of receiving 402-type data sets.
16	C Connector	Connected to data set during testing of transmitting 402-type data sets.
17	TEST MODE Switch	Determines output of eight parallel data channels.
18	TRMT CLOCK PHASE Switch	Determines relationship of clock and data signals for parallel data set tests.

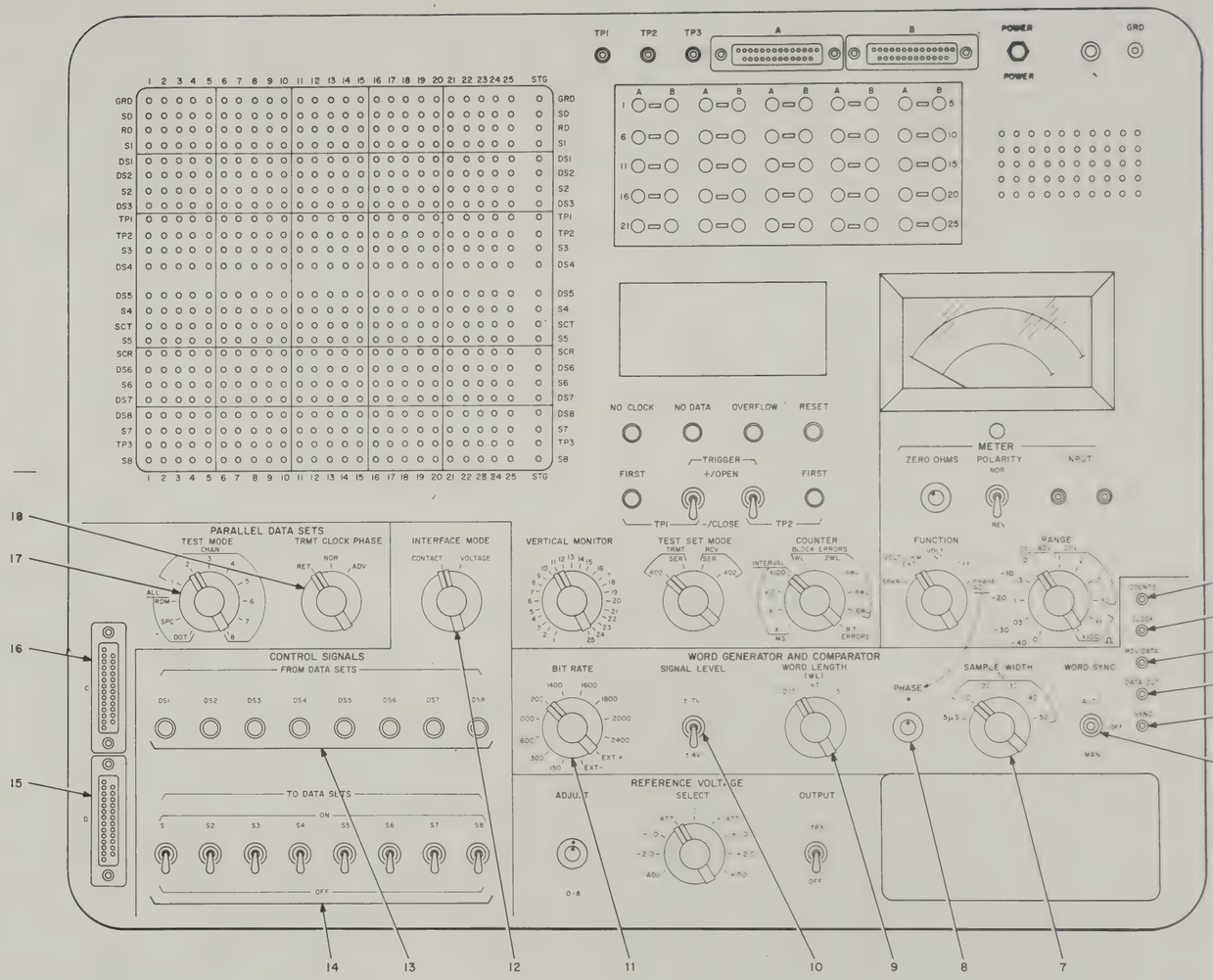

Fig. 6—914B Data Test Set—Controls and Indicators (C)

3. FUNCTIONAL DESCRIPTION

3.01 For a functional descripton of the 914B Data Test Set, four major block diagrams are required. These four block diagrams are shown in Fig. 7, 8, 9, and 10, and represent (a) the overall function of the 914B, (b) the serial transmit and receive function, (c) the parallel data transmit, and (d) the parallel data receive functions.

Overall Function (Figure 7)

3.02 Data sets to be tested are connected to the 914B Data Test Set via connectors A or B (connectors C or D for 402-type data sets). The leads of these connectors link through the interface selector switches to the vertical buses of the program matrix. With both the A and B sections of a particular interface selector switch closed, the corresponding pins of connectors A and B are interconnected. In the most common tests of a data set, either connector may be used to connect the data set interface to the test set.

3.03 Under some circumstances, it may be desirable to test a data set on an in-service basis, ie, with the business machine connected to the data set. In a test of this nature, connector A is connected to the data set and connector B to the business machine. When the A and B sections of the interface selector switch are closed, the signals passing through the data set/business machine interface are accessible on the program matrix in a bridging connection. By opening and closing the respective A and B sections of the interface selector switches of individual interface leads, access to the data set or business machine interface may be obtained, breaking the connection between the data set and the customer interface.

3.04 The program matrix is a 2-deck array of 25 vertical and 24 horizontal buses. The vertical buses are connected to the interface leads of the data set, while the horizontal buses connect to the various test circuits in the 914B. Interconnections are made by inserting a programming (shorting) pin at the intersection of the corresponding vertical and horizontal buses. Plugs having built-in resistances can be used when it is desired to make a connection through a series resistance.

3.05 Eight of the horizontal buses of the program matrix carry control signals from the 914B. The signals are controlled by toggle switches S1 through S8. These signals are either ± 4 volt voltage levels or contact closures depending on the position of the INTERFACE MODE switch.

3.06 Lamps DS1 through DS8 indicate the presence of control signals on their respective eight horizontal buses of the matrix. With the INTERFACE MODE switch in the CONTACT position, a contact closure to ground on a horizontal bus lights the corresponding indicator lamp. When the INTERFACE MODE switch is in the VOLTAGE position, a $+4$ volt signal present on a horizontal bus activates the respective lamp driver which in turn lights the corresponding lamp.

3.07 The first horizontal bus supplies ground to the matrix. TP1, TP2, and TP3 buses are accessible at test points on the front panel of the 914B. Additionally, TP1 and TP2 are connected to the interval counter circuit. TP3 is also connected to the reference voltage when the OUTPUT switch is set to TP3.

3.08 The SD and RD buses carry the send and receive data signals when the TEST SET MODE switch is in the TRMT or RCV position. Similarly, the SCT and SCR buses carry the transmit and receive clock signals.

3.09 Each of the 25 interface leads is shunted by a 300-kohm resistor to provide marginal open-circuit loading for contact interfaces.

3.10 The VERTICAL MONITOR switch connects to the dc voltmeter and facilitates dc voltage measurements on any of the interface leads of the data set being tested.

3.11 The meter circuit permits the measurement of dc voltage, ac voltage, resistance and signal level in dBm (referenced to a 600-ohm load.) In addition, it makes possible monitoring of line signals with a loudspeaker. The dc signals to be measured may be applied to the metering circuits by means of the VERTICAL MONITOR switch or from INPUT terminals on the front of the test set. The ac volts, ohms, and loudspeaker signals may be applied to the metering circuits only from the METER INPUT jacks. The type of signal to be measured determines the required position of the FUNCTION switch.

3.12 The reference voltage circuit develops fixed voltages of $+7$, ± 2, ± 1, and ± 0.477 volts.

In addition, a voltage adjustable over the range of 0 to +8 volts is available. The voltage is selected by the SELECT switch and may be applied through the OUTPUT switch to the TP3 jack or the TP3 horizontal matrix buses for use in testing analog type data sets.

3.13 The interval counting circuits monitor the state of two leads, TP1 and TP2, and recognize the one on which a preselected signal first occurs. This signal, depending on the position of the TRIGGER switch, may be a positive or negative transition or a contact opening or closing. The circuit also permits the measurement of the time interval between the signal occurrences on the two leads. The functions to be measured can be connected by using the TP1 and TP2 jacks on the front panel of the test set or the TP1 and TP2 horizontals in the program matrix. The occurrence of the preselected signals is indicated by the FIRST TP1 or FIRST TP2 lamp. The time interval is read out on the counter display. Time intervals from 0.1 ms to 10 seconds may be measured.

Serial Transmit and Receive Function (Figure 8)

3.14 Timing control for the clock is determined by the position of the BIT RATE switch. The basic clock circuit is used in both the transmit and receive modes. In the receive mode the bit sync recovery circuit generates signals which are used to drive the clock circuit at a rate determined by the incoming data signal. The PHASE control is adjusted to achieve precise synchronism with the incoming data signal. With the BIT RATE switch set to EXT, timing is supplied by the data set clock. The clock signal (either internally generated or external) is simultaneously applied to the word generator and the sample pulse generator.

3.15 The word generator produces three different digital test messages under control of the WORD LENGTH switch:

(a) Dot signal, ie, alternate marks and spaces

(b) 63-bit test word

(c) 511-bit test word.

The bit rate, established by the applied clock signals, must be in the range from 10 to 20,000 bits per second.

3.16 The word sync circuits provide synchronization between the locally generated word and the received data word. These two words are identical except for discrepancies due to transmission impairments or malfunctions in the data sets under test. Word synchronization is accomplished either manually or automatically, depending on the position of the WORD SYNC switch. The manual sync mode is initiated by momentarily operating the spring-loaded WORD SYNC switch to the MAN position. In the comparator a bit-by-bit comparison is made between the received word and the locally generated word and differences are read out as errors on the counter display.

3.17 When the 914B is used in a manual synchronous mode, (WORD SYNC switch momentarily set to MAN) the comparator and word generator are synchronized with the data set output on the first available information bit. Random noise may cause loss of synchronization resulting in an extremely high error rate, indicated by a counter display overflow. Automatic synchronization (WORD SYNC switch set to AUTO) causes the test set to resynchronize with every information bit, resulting in a nominal error count and indicating the presence of random noise pulses. With the WORD SYNC switch in the AUTO position the error count displayed is approximately three times the true error count.

3.18 The sample pulse generator normally provides a 0.5 μsec sampling pulse centered in the midbit position. For testing asynchronous data sets there are additional variable sampling widths available, which allow the sampling interval to be adjusted in 10-percent steps from 10 to 50 percent of the bit interval by the SAMPLE WIDTH switch. This provides a means of indicating the data error signal margin. Any discrepancy between a received bit and the corresponding locally generated bit during a sampling interval is registered as an error.

3.19 The error counting circuit will indicate the average bit error rate or the block error rate of the system. In the block error mode, the number of blocks of a certain length containing one or more errors is counted. The block lengths are multiples of the word length, ie, 63 or 511 bits. The multiples are 1, 2, 4, 8, and 16, as selected by the COUNTER switch.

3.20 The EIA output driver conditions the locally generated word for application to the SD lead to drive a transmitting data set in an end-to-end test.

Parallel Data Transmit Circuits (Fig. 9)

3.21 The clock signal generated by the transmit clock multivibrator is applied to the dot generating circuits. The clock signal is a 75-Hz signal and the dotting signals are 75 bps.

3.22 One of the dot signals under control of the TRMT CLOCK PHASE switch is applied to the timing channel of the parallel data set. This signal may, by the use of the ADV or RET switch, be advanced or retarded in phase by 1.5 ms with respect to the data signal. This is used to simulate a change in phase relationship between the clock and data signals that might occur due to transmission impairments.

3.23 The signal from the data dot generator in combination with the test word is applied to some of the eight parallel data channels. The TEST MODE switch determines the output of the eight parallel data channels, allowing the channels to be tested individually or simultaneously. With the TEST MODE switch in the ALL DOT position, all data channels are driven by the dot generator which provides a signal of alternate marks and spaces. An ALL SPC (constant spacing signal) may also be applied to the data channels. Other positions of the TEST MODE switch allow applying the test word to all channels (ALL RDM) or to any individual channel (CHAN/1-8), while the remaining channels carry a dot signal.

3.24 The output drivers provide the contact closure type interface required for Data Sets 402-type. All data channels and the timing channel are accessible through the C connector on the front panel.

Parallel Data Receive Circuits (Fig. 10)

3.25 The receiving parallel data set is connected to connector D on the front panel. The receiving data channels may be tested individually or simultaneously under control of the TEST MODE switch. When the data channels are tested on an individual basis, the received data signal is checked for errors as described previously in this section.

3.26 When all channels are tested simultaneously (ALL RDM position of the TEST MODE switch), the test word is transmitted on all channels by the transmitting data set. The inputs from all channels are combined and compared to the local word from the word generator. If one or more channels are in error, an error signal is fed to the data comparator and registers as an error on the COUNTER display.

3.27 The timing signal on the parallel receive data timing channel is applied to the level converter and eventually to the external clock input of the local word generator.

Power Supply

3.28 The power supply produces all of the voltages required by the circuits of the test set. It converts 115-volt 60-Hz power into three regulated dc outputs of +12, −12, and +5 volts and two unregulated outputs of +23 and +200 volts.

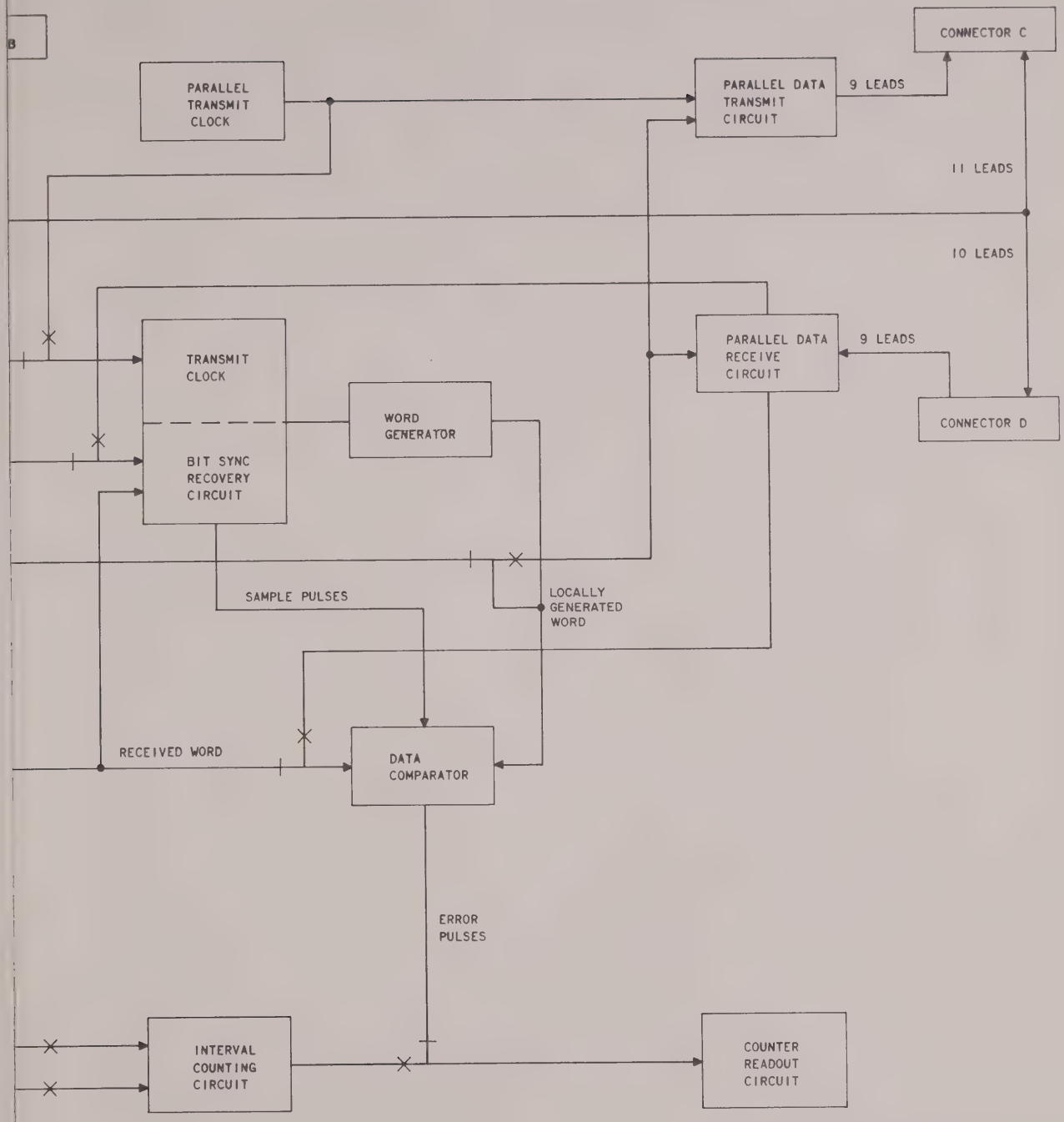

Fig. 7—914B Data Test Set—Overall Functional Block Diagram

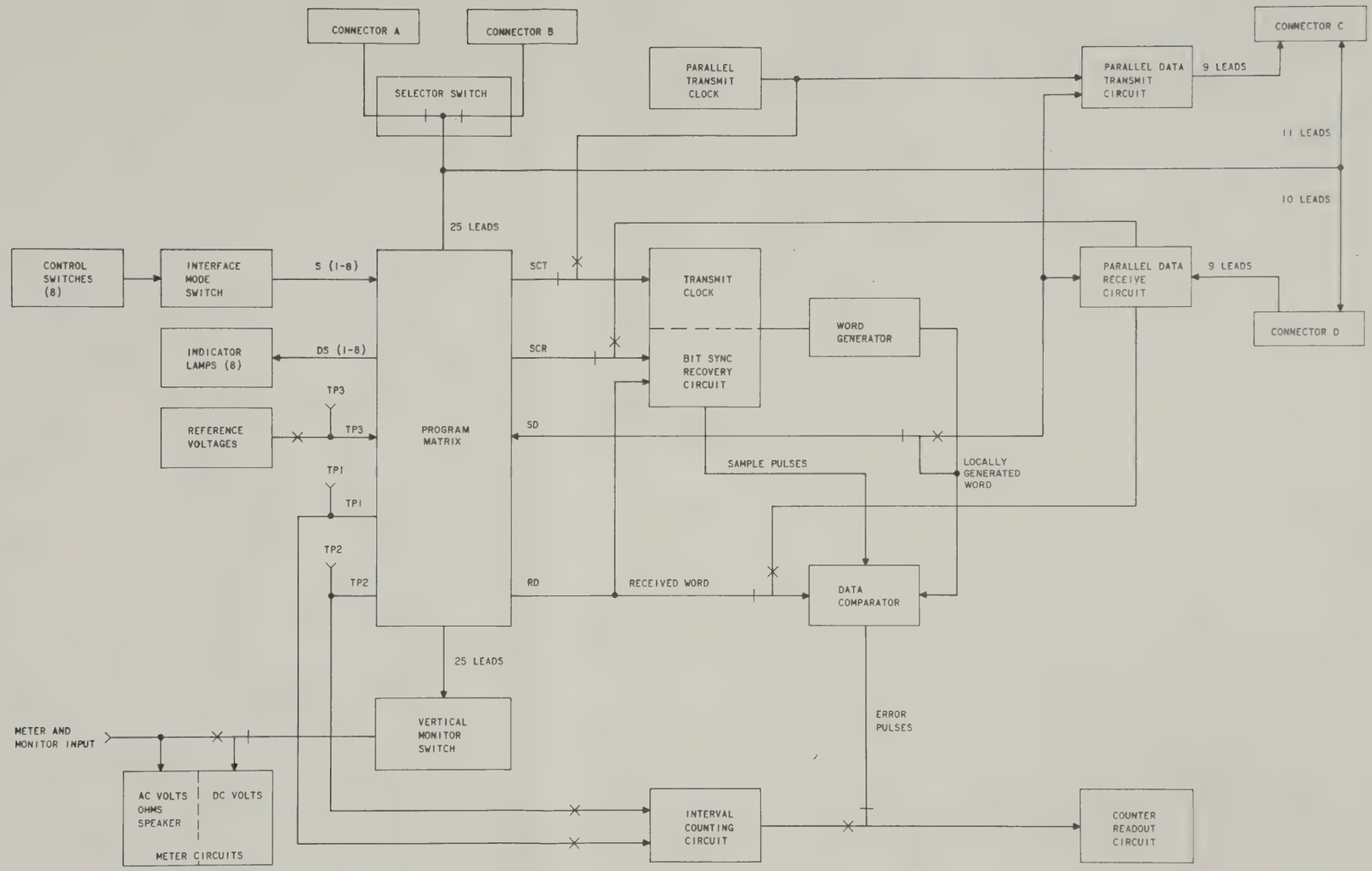

Fig. 7—914B Data Test Set—Overall Functional Block Diagram

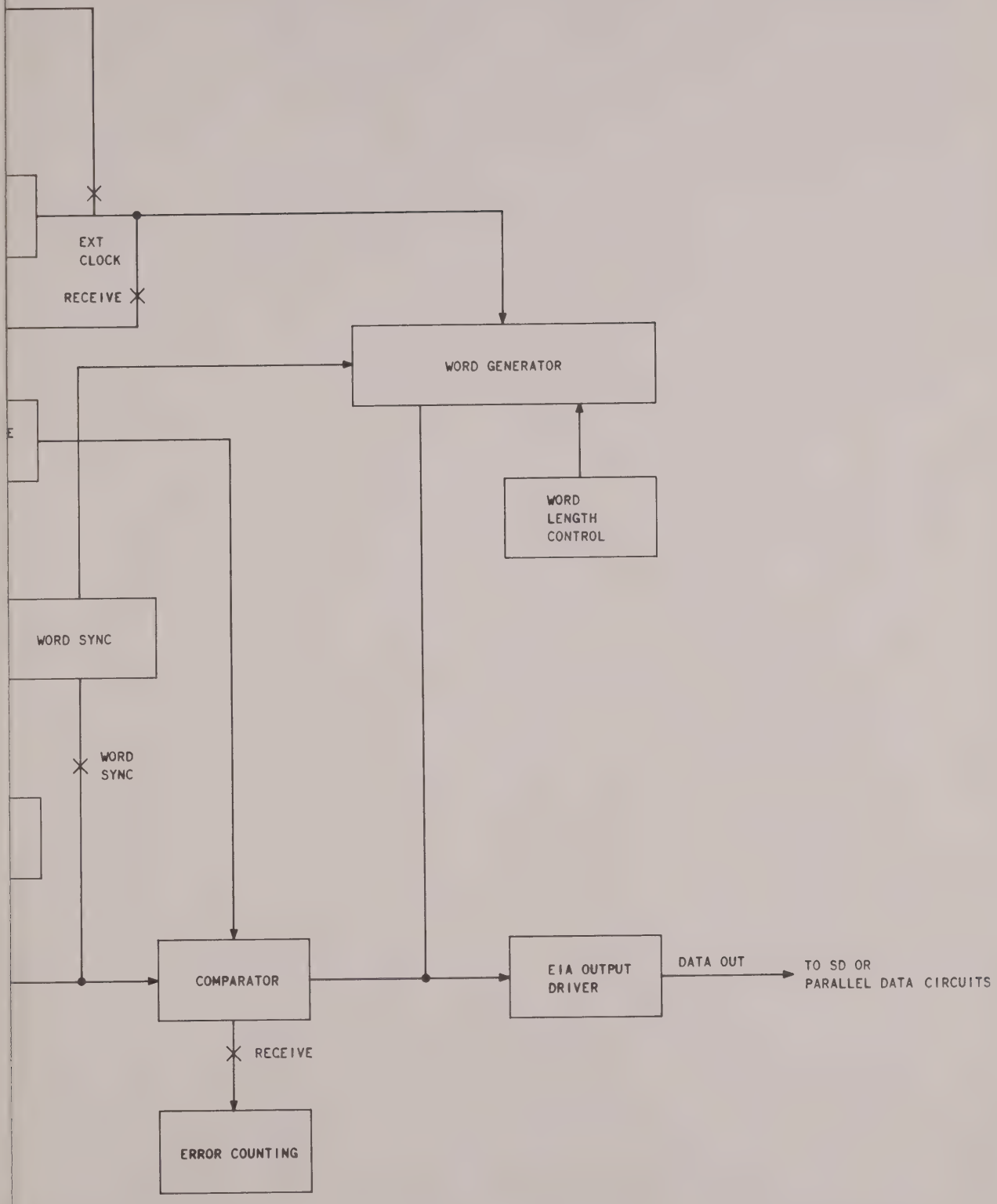

Fig. 8—914B Data Test Set—Serial Transmit and Receive Circuits

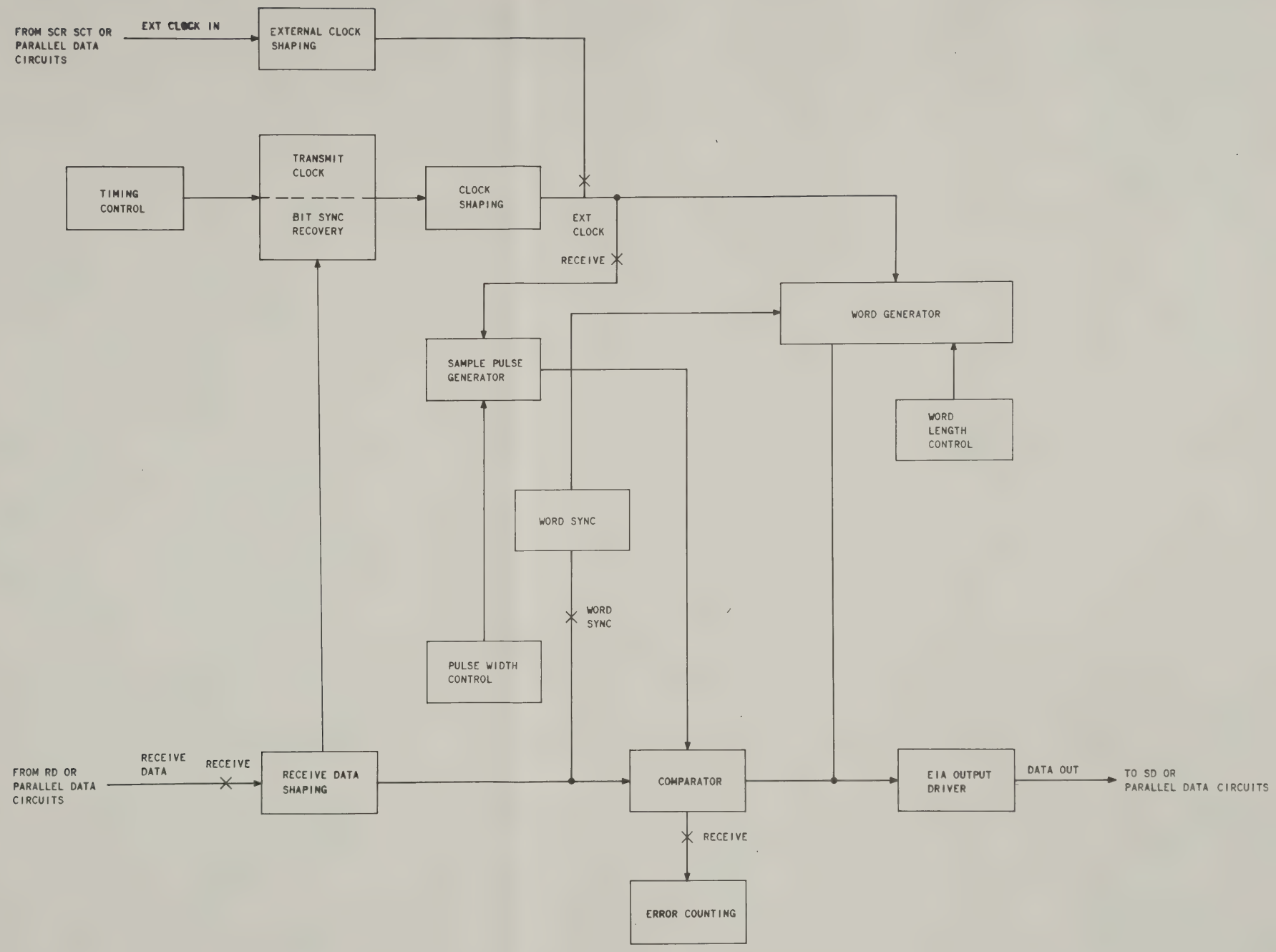

Fig. 8—914B Data Test Set—Serial Transmit and Receive Circuits

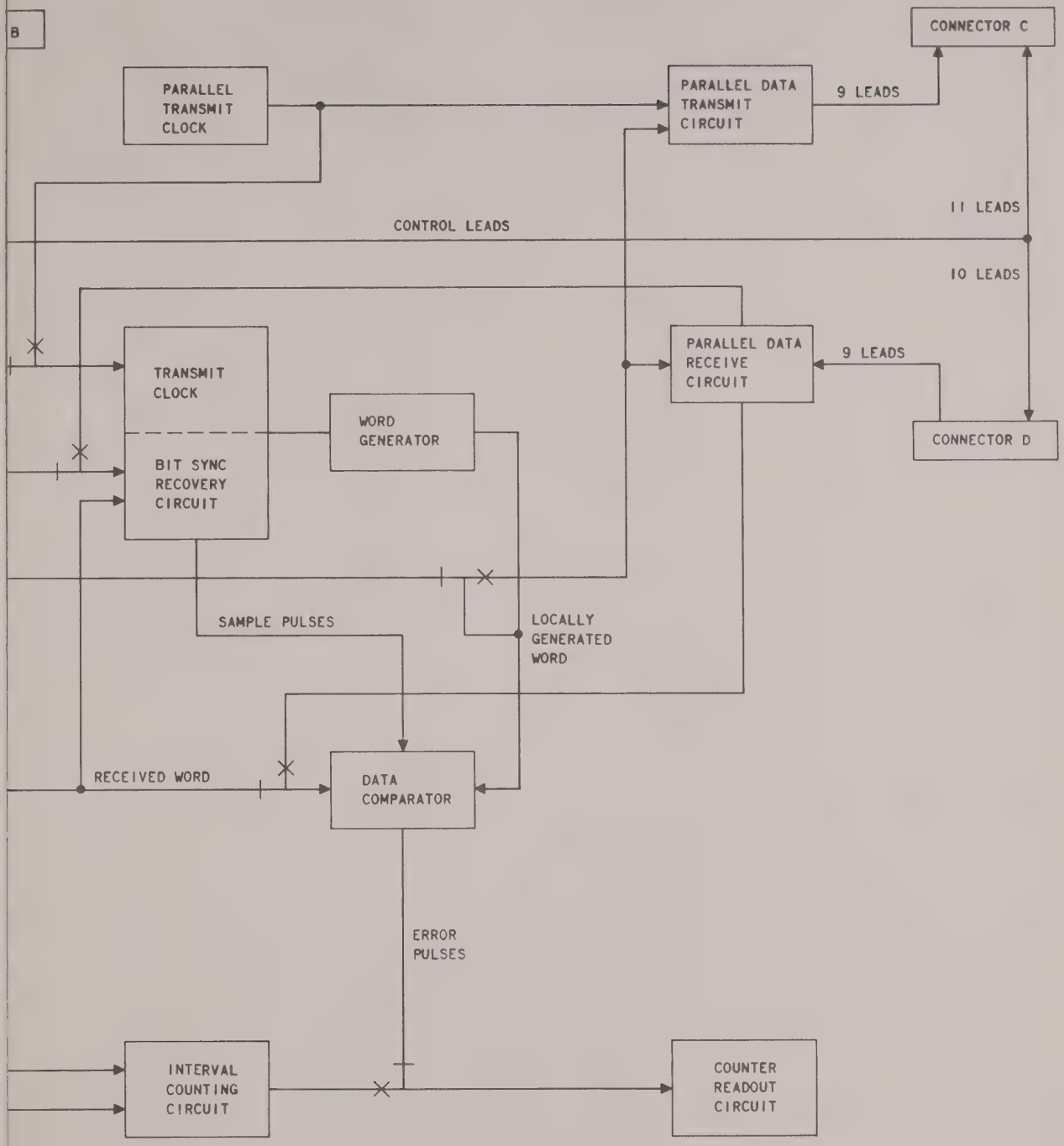

Fig. 9—914B Data Test Set—Parallel Data Transmit Circuits

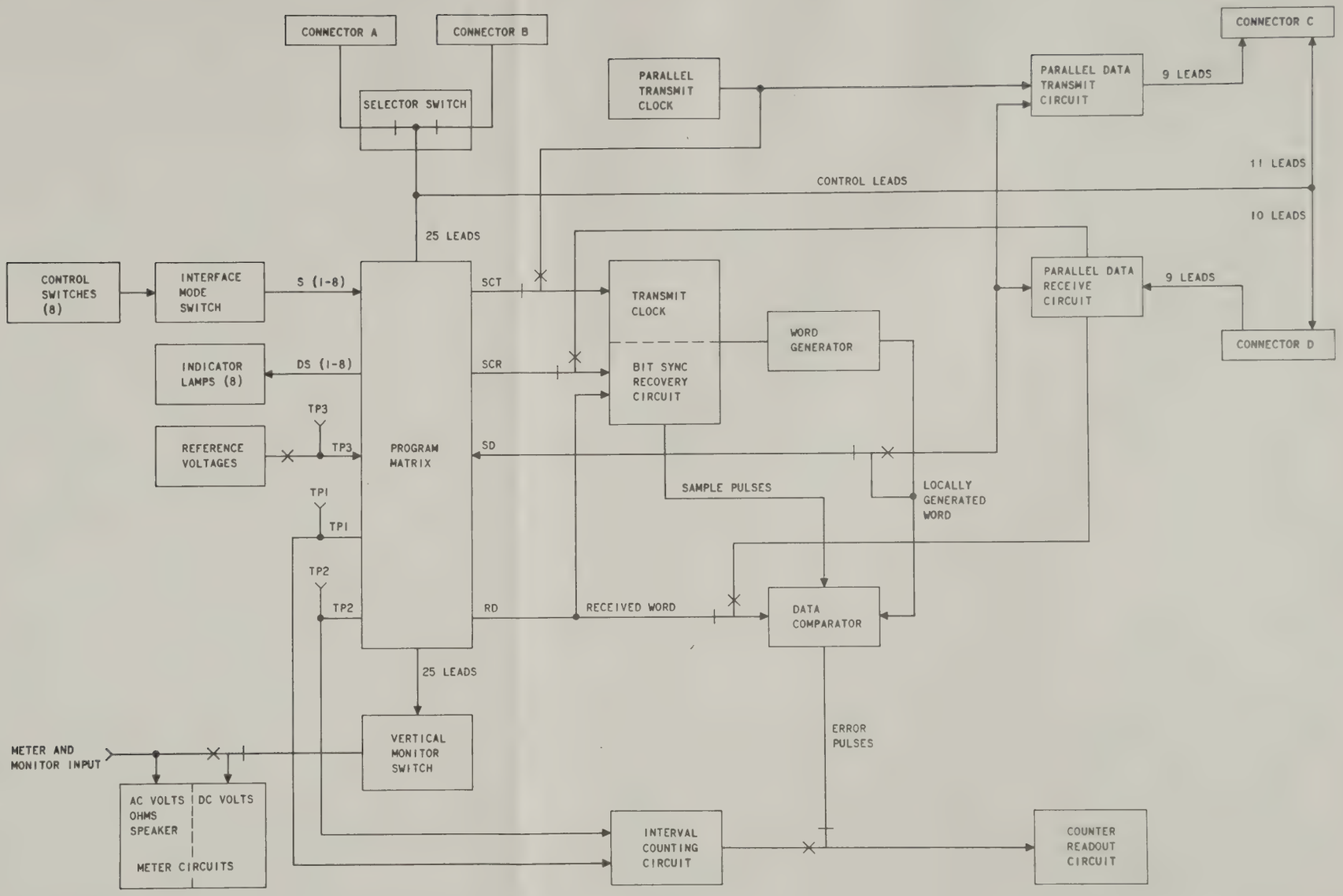

Fig. 9—914B Data Test Set—Parallel Data Transmit Circuits

4. OUTPUT SPECIFICATIONS AND INPUT REQUIREMENTS

4.01 The signal outputs of the 914B Data Test Set are accessible at the program matrix and the various test points on the front panel. Table D lists these outputs and their characteristics.

4.02 The input requirements of the 914B are shown in Table E.

TABLE D

OUTPUT SPECIFICATIONS

OUTPUT	CHARACTERISTIC
SD	Bi-polar, NRZ (nonreturn to zero) signal ±3.5 to ±5 volts or ±0.7 volt in amplitude from an impedance of 200 ohms with rise and fall times not exceeding 1 μsec.
S1-S8 CONTROL SIGNALS	±3.5 to ±5 volt dc levels in the voltage mode, contact closures to ground and open circuits in the contact mode.
REFERENCE VOLTAGES	+7, ±2, ±1, ±0.477 volts dc within ±1 percent of specified value; the ±1 and ±2 volt outputs are balanced within ±0.5 percent. Maximum source resistance 330 ohms.
COUNTS	A pulse issued for every 100 errors recorded on the internal counter; +4 volt amplitude, 70 μsec width, from a resistance of 3500 ohms.
CLOCK	A symmetrical square wave +4.5 volts in amplitude, frequency equal to the bit rate of the test set. The positive clock transitions coincide with the transitions of the generated data signal.
RCV DATA	In the SER RCV mode the signal applied to the RD horizontal of the program matrix appears on this test point. In the 402 RCV mode the bi-polar ±6 volt output of the level converter is present on this test point.
DATA OUT	The bi-polar data signal produced by the word generator; ±4 volts or ±0.7 volt in amplitude, as selected by the SIGNAL LEVEL switch.
SYNC	A positive pulse, one bit interval in length, occurring once per word. The amplitude is 4.8 volts from a resistance of 1000 ohms.

TABLE E

INPUT REQUIREMENTS

INPUT	REQUIREMENT
RD	Bi-polar NRZ (non-return to zero) signal, minimum amplitude ±3 volts; input resistance 2400 ohms in series with a silicon diode junction.
SCR	Bi-polar square wave, minimum amplitude ±3 volts; input resistance 2400 ohms in series with a silicon diode junction.
SCT	Same as SCR.
DS1-DS8 VOLTAGE MODE	+3 volts dc level to light lamp; input resistance 3000 ohms in series with a silicon diode junction.
DS1-DS8 CONTACT MODE	Contact closure to ground to light lamp; lamp current 40 mA, lamp voltage +23 volts.

5. OPERATIONS AND TYPICAL TEST ARRANGMENTS

5.01 The intent of Part 5 is to give general information on testing which will allow the user to better understand the use of the test set. It should be noted that the tests in this section make use of the 914B on both the transmitting and receiving ends (Fig. 11, for example). However, tests using the 914B and another data test set such as a 901, 902, 903, 913, or data test center, are possible and should be considered. Test procedures shown in this part are typical for serial, parallel, and analog types of data sets and will specify switch settings, connections, operating instructions and any additional test equipment required. For detailed instructions for test of a particular data system, refer to the appropriate test section.

5.02 ***Matrix:*** The most unique feature of the 914B Data Test Set is the programmable matrix which provides flexibility in connecting the test circuits to the interface leads. In most tests, the data set is connected to connector A via a furnished cable. This connects the data set interface leads to the vertical buses of the matrix. Appearing on the horizontal buses of the matrix are the inputs and outputs of test circuits contained in the 914B. Shorting pins (red), when inserted in the matrix face, connect the desired horizontal and vertical buses. Resistance pins are also provided which make the connection through an internal resistance in the pin (gray pins 10 ohms, green pins 18 ohms). The assignment of the input-output leads to the horizontal buses is such that in general the location of the programming pins will be along the diagonal of the matrix face. Figure 12 shows the matrix programmed for testing Data Set 202D. It can be seen that the send request (SR) lead is connected to S1 switch so that the send request function is controlled by S1. The clear-to-send (CS) signal, located on pin 5 of the interface, is connected to the DS-1 lamp; therefore, DS-1 provides an indication of the CS signal from the data set. The send data (SD) lead is connected to the SD bus on the matrix which carries the word generator output. Similarly, receive data (RD) appears on pin 3 of the matrix and is connected to the comparator circuits when the test set is in the receive mode. To measure the 202D power supply voltage appearing on pins 9 and 10 (or any other dc voltage) the meter FUNCTION switch must be set to INT and the VERTICAL MONITOR switch set to the desired number of the interface lead.

5.03 ***Selector Switch:*** The interface selector switch shown in Fig. 13 consists of an A and B section, each of which is a combination switch and test point. When both A and B switches are closed, the respective pins (pin 1, for example) on

Fig. 11—Typical Test Arrangement for End-to-End Testing with 914B Data Test Sets

202D DATA SET EIA LEAD DESIGNATIONS

	1 FG	2 SD	3 RD	4 SR	5 CS	6 DSR	7 SG	8 CF	9	10	11 STD	12 SRD	13	14	15	16	17	18	19 RR	20 DTR	21 RDY	22 RI1	23 RI2	24	25	STG	
GRD	●	o	o	o	o	o	●	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	GRD
SD	o	●	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	SD
RD	o	o	●	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	RD
SI	o	o	o	●	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	SI
DSI	o	o	o	o	●	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	DSI
DS2	o	o	o	o	o	●	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	DS2
S2	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	S2
DS3	o	o	o	o	o	o	o	●	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	DS3
TPI	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	TPI
TP2	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	TP2
S3	o	o	o	o	o	o	o	o	o	o	●	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	S3
DS4	o	o	o	o	o	o	o	o	o	o	o	●	o	o	o	o	o	o	o	o	o	o	o	o	o	o	DS4
DS5	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	DS5
S4	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	S4
SCT	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	SCT
S5	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	S5
SCR	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	SCR
DS6	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	●	o	o	o	o	DS6
S6	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	●	o	o	o	o	o	o	o	S6
DS7	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	●	o	o	o	o	o	o	DS7
DS8	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	●	o	o	o	DS8
S7	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	●	o	o	o	o	o	S7
TP3	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	TP3
S8	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	S8
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	STG	

Fig. 12—Matrix Programmed for Data Set 202D

connectors A and B are connected to A1 and B1 test points and also to the test point located between the switches. By proper use of the interface selector switches, each lead of the A and B connectors may be connected in a bridging or terminating mode for testing on an in-service basis. This flexibility also allows testing of data sets having up to 50 interface leads.

5.04 ***Meter:*** A volt-ohm-meter is an integral part of the 914B and may be used to monitor dc interface signals by placing the FUNCTION switch in the VOLT INT position, selecting the proper RANGE switch setting and operating the VERTICAL MONITOR switch to the position corresponding to the desired vertical lead.

5.05 External circuits may be monitored by attaching test leads to the INPUT terminals and setting the FUNCTION switch to the VOLT/OHM EXT position. In this position ac signals, dc voltages and resistance to ground may be measured.

One side of the ohmmeter is permanently grounded to the 914B, therefore, all readings are taken with respect to test set ground.

5.06 The ac meter input is a balanced high impedance circuit so that the meter may be connected to a telephone line with negligible loading effect.

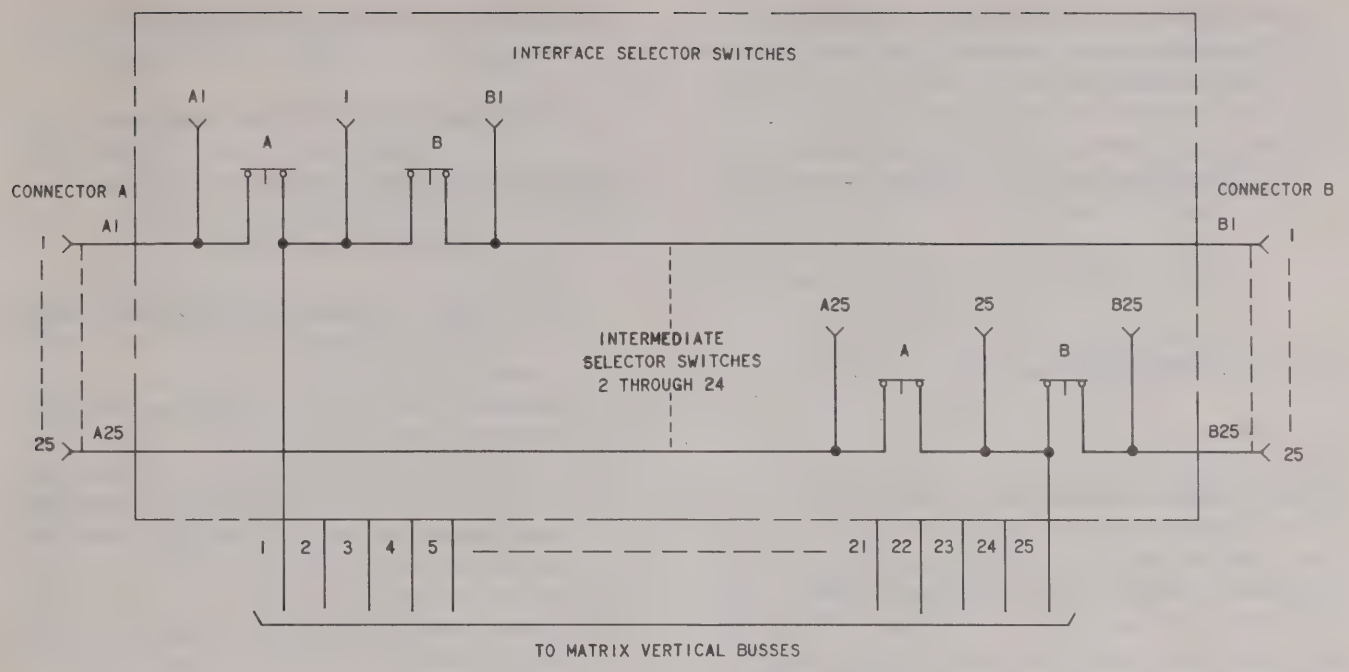

Fig. 13—A and B interface Selector Switches—Schematic

Damage may result to the meter when measuring line signals (FUNCTION switch set to EXT) if the RANGE switch is inadvertently placed in the DCV or X1, X100 (ohms) position. The FUNCTION switch should be set to OFF when the meter is not being used or when the test set is being transported.

5.07 With the FUNCTION switch set to SPKR and the RANGE switch set to any of the ACV positions, ac signals applied to the INPUT terminals are audible in the loudspeaker. The loudspeaker volume is controlled by setting the RANGE switch to any of the five ACV positions.

5.08 ***Interval Counter:*** The 914B contains an interval counter circuit which monitors the state of the TP1 and TP2 leads. The circuits function to detect and provide a lamp indication of the first occurrence of a preselected signal on either TP1 or TP2 leads. The lead on which the signal first occurs results in lighting either the FIRST TP1 or the FIRST TP2 lamp. In addition, time between signals and signal duration may be measured using the counter display. The signals to be monitored may be either a positive or negative voltage transmition or the closing or opening of a contact. By setting the TRIGGER TP1 and TRIGGER TP2 switches to detect the proper signal transition, the time interval between pulses on the two leads may be read out on the display counter. The duration of a single pulse may be measured by applying the same signal on both TP1 and TP2 leads and setting the TRIGGER TP1 and TRIGGER TP2 switches to detect the plus and minus transitions of the pulses respectively. The interval measured is the width of the pulse.

5.09 Signals to be measured may be applied to the interval counter circuits in two ways: (a) from the TP1 and TP2 horizontal matrix buses or (b) from the TP1 and TP2 test points on the front of the test set. The following controls and indicators are used with the interval counting circuits:

COUNTER—Set to desired time interval.

BIT RATE—Set to any of the interval bit positions.

TEST SET MODE—Set to TRMT SER.

TRIGGER, FIRST TP1 and FIRST TP2 switches—set in accordance with type of signal to be detected (+/OPEN or −/CLOSE).

TRIGGER FIRST TP1 and FIRST TP2 lamps—Indicate on which lead the preselected signal first occurs.

RESET—Operate momentarily to clear count.

Display counter—Read duration interval when event occurs.

Serial Data Sets

5.10 Connect the data set to be tested to the A or B connector and ensure that the matrix has been programmed for the data set under test. Set the INTERFACE MODE switch to VOLTAGE or CONTACT as required (normally VOLTAGE for serial data sets). Set switches S1 through S8 to properly condition the data set. Observe indicator lamps DS-1 through DS-8 for the proper indication.

5.11 Interface voltage measurements are made by setting the meter FUNCTION switch to VOLT INT and the RANGE and POLARITY switches to the proper position. The VERTICAL MONITOR switch may be set to any one of the 1 through 25 positions to monitor the dc voltages on the interface leads. ***The NO DATA and NO CLOCK indicator lamps should remain extinguished during all error rate tests unless a data or clock malfunction occurs. The data or clock signal must be absent for several seconds for the lamps to illuminate.***

5.12 Controls and switch settings listed under the following three headings are used when testing all types of serial data sets in transmitting and receiving modes.

Transmitting Tests—Synchronous or Asychronous Data Sets

TEST SET MODE—Set to TRMT SER.

BIT RATE—Set to appropriate BIT RATE for asynchronous data sets. Set to EXT+ or EXT− for synchronous data sets, depending on phase relationship of clock signal to data signal (normally EXT+).

SIGNAL LEVEL—Set to ±0.7V or ±4V as required.

WORD LENGTH—Set to desired test signal.

Receiving Tests—Synchronous Data Sets

TEST SET MODE—Set to RCV SER.

COUNTER—Set to BIT ERRORS or BLOCK ERRORS as required.

WORD LENGTH—Set to agree with transmitted word.

BIT RATE—Set to EXT+ or EXT−, depending on phase relationship of clock signal to clock signal (normally EXT+).

WORD SYNC—Operate momentarily to MAN or set to AUTO.

RESET—Operate momentarily to clear counter.

Counter display—Observe recorded error count.

Receiving Tests—Asychronous Data Sets

TEST SET MODE—Set to RCV SER

COUNTER—Set to BIT ERRORS or BLOCK ERRORS as required.

WORD LENGTH—Set to agree with transmitted word.

PHASE—Set to mid position (dot pointing up).

BIT RATE—Set to agree with transmitted bit rate.

FUNCTION—Set to PHASE ADJ.

PHASE—Adjust for null on METER.

FUNCTION—Set to position other than PHASE ADJ (do not return to PHASE ADJ during remainder of test).

SAMPLE WIDTH—Set to ◗.5μS◖.

WORD SYNC—Operate momentarily to MAN or set to AUTO.

SAMPLE WIDTH—Set to desired sampling interval for marginal testing.

RESET—Operate momentarily and observe recorded error count on counter display.

Parallel Data Sets—402-Type

5.13 Connect the data set to be tested to the C (transmit) or D (receive) connector and ensure that the matrix has been programmed for the data set under test. Set the INTERFACE MODE switch to the CONTACT position. Set switches S1 through S8 to properly condition the data set. Observe indicator lamps DS-1 through DS-8 to ascertain that the data set is responding properly. To test for interaction between any particular data channel and other data channels set the TEST MODE switch to the desired channel (CHAN 1 through 8). Setting the TEST MODE switch to the ALL SPC position applies a spacing condition to all data channels; the ALL DOT position applies alternate marks and spaces to all channels. ***The NO DATA and NO CLOCK indicator lamps should remain extinguished during all error rate tests. A NO DATA lamp indication indicates a trouble condition, not necessarily a lack of data.***

5.14 Controls and switch settings listed under the following two headings are used when testing all 402-types of parallel data sets in transmitting and receiving modes.

Transmitting Tests

WORD LENGTH—Set to 63 or 511 bits as required.

SIGNAL LEVEL—Set to $\pm$4 volts.

BIT RATE—Set to EXT+.

TEST SET MODE—Set to TRMT 402.

TEST MODE—Set to ALL RDM to test all eight channels individually or simultaneously.

TRMT CLOCK PHASE—Set to RET, NOR, or ADV as required. In an end-to-end test this control at the transmitting data test set may be set to the ADV or RET position, which will change the phase relationship between the clock signal and the data signal by 1.5 msec. This establishes a marginal condition which will normally result in increased errors at the receiving data set.

Receiving Tests

TEST SET MODE—Set to RCV 402.

COUNTER—Set to BIT ERRORS or BLOCK ERRORS as required.

TEST MODE—Set to ALL RDM to test all eight channels simultaneously. Set to CHAN/1-8 to check any channel individually.

WORD SYNC—Operate momentarily to MAN or set to AUTO.

RESET—Operate momentarily to clear counter.

Counter display—Observe recorded error count.

Analog Data Sets

5.15 Precision reference voltages generated by the 914B may be used to make tests on analog data sets. Generally the procedure is to program the matrix, set switches S1 through S8, apply a known voltage to the SD lead of the transmitting data set and measure the voltage on the RD lead at the receiving data set. The voltmeter is used to measure the signal on the RD lead. At the transmitting end, the voltage may be applied to the TP3 bus on the matrix by setting the OUTPUT switch to TP-3. The voltage may then be monitored with the meter through contacts of the VERTICAL MONITOR switch.

Transmitting Tests—Analog Data Sets

REFERENCE VOLTAGE—Set to desired voltage or ADJ position.

OUTPUT—Set to TP3. Insert programming (shorting) pin at matrix intersection of TP3 horizontal bus and SD lead.

VERTICAL MONITOR—Set to monitor interface SD lead, using meter circuit.

- ADJUST—Adjust to the desired voltage, using meter circuit when REFERENCE VOLTAGE switch is set to ADJ.

Receiving Tests—Analog Data Sets

- VERTICAL MONITOR—Set to monitor interface RD lead, using meter circuit. Meter indication should agree in magnitude and polarity with transmitted voltage.

6. MAINTENANCE

6.01 Maintenance tests in this section should be performed in accordance with local instructions. Maintenance and repair of the 914B in the field should be limited to the replacement of fuses, lamps and calibration of the ac voltmeter. Some tests are provided in this section which will aid the user in determining if the test set is operating within tolerances, and to isolate minor malfunctions to a particular lamp or fuse which needs replacement. In some instances it may be possible to isolate the trouble to one or more of the six replaceable circuit packs. Replacement circuit packs are available but must be ordered separately. Repairs beyond those mentioned above should be referred to the appropriate Western Electric Company organization.

6.02 The 914B has features which permit self-testing of most of its functions without the use of additional test equipment. Part 6 provides test methods which will give an indication of the operational status of the test set. Certain of the tests are general in nature and should not be considered conclusive.

THINK

Before proceeding with any test in this section, ensure that all test leads and matrix pins have been removed, all interface selector switches are depressed, all interface connecting cables are free of shorts, opens and crosses, ▸and the FUNCTION switch is in the OFF position.◂

6.03 To gain access to R17 (for ac voltmeter calibration), fuses, and circuit packs, it is necessary to remove the rear cover of the test set. This is done by loosening the four quick release fasteners at the rear of the test set. With the test set front panel facing up, lift the test set chassis out of the case. Figure 14 shows the locations of the test set fuses. Figure 15 provides information for circuit pack location and R17.

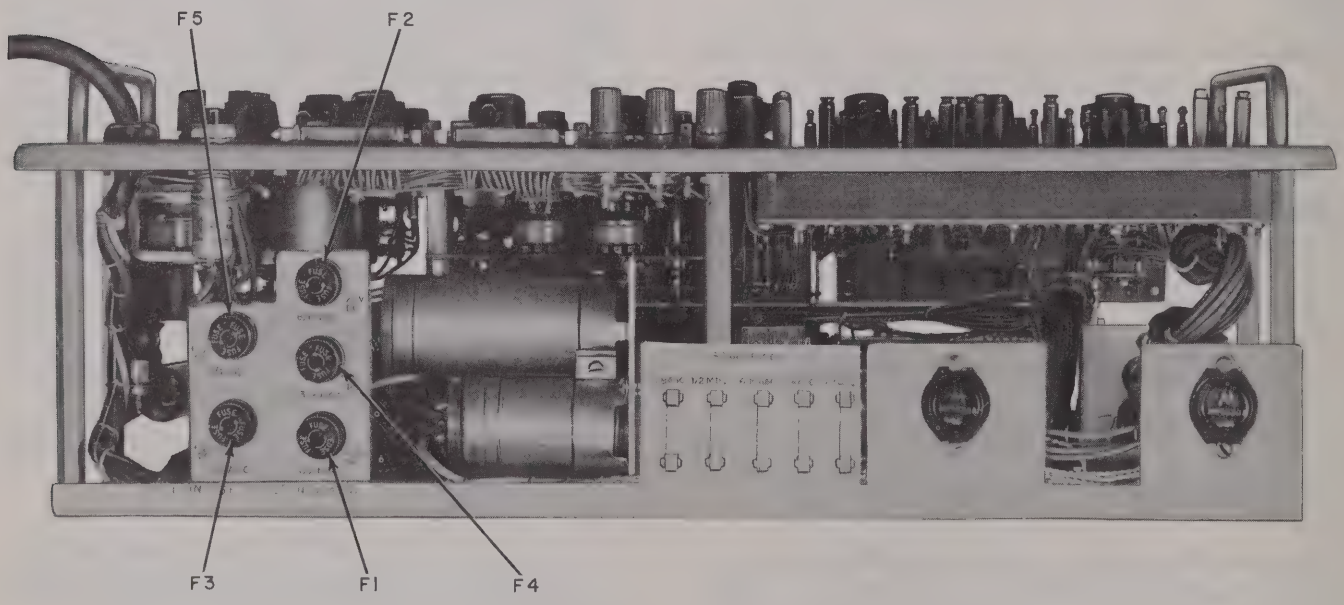

Fig. 14—914B Data Test Set—▸Fuse Location◂

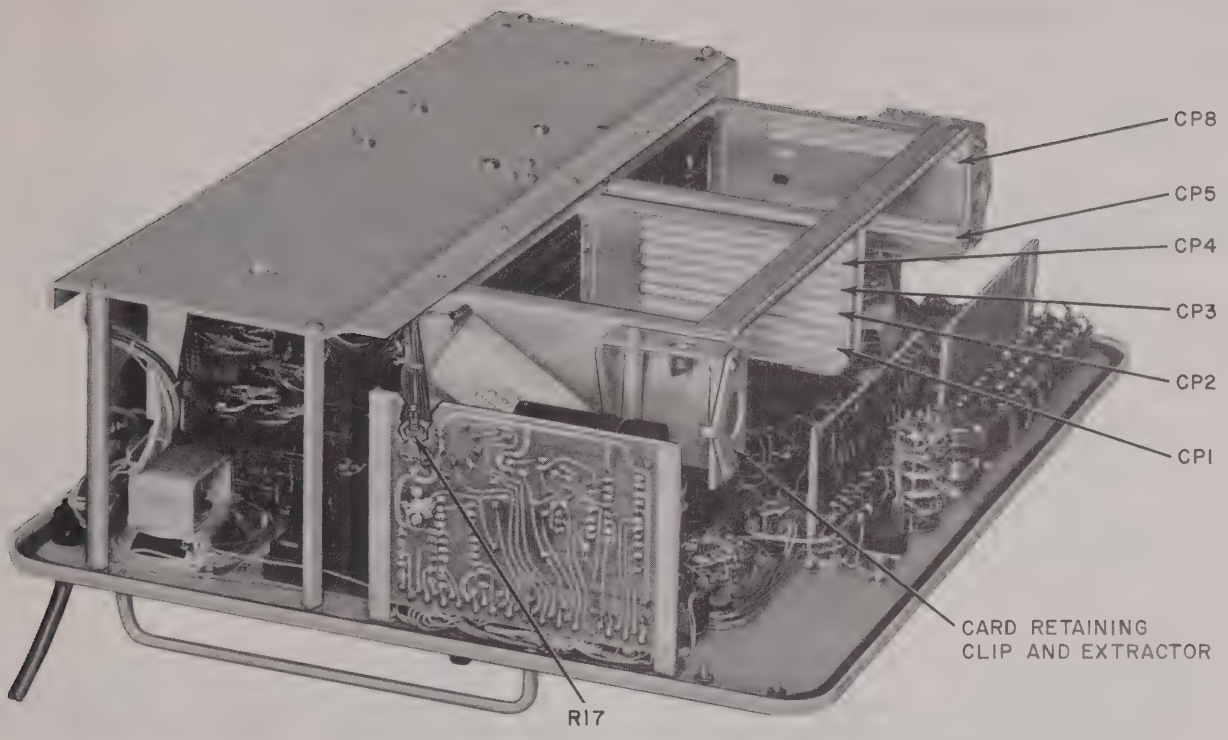

Fig. 15—914B Data Test Set—Circuit Pack and AC Calibration Location

6.04 Test procedures in 6.05 through 6.10 permit testing the 914B without additional test equipment or another 914B. Tests in 6.11 through 6.15 require additional equipment.

THINK ***Circuit pack and lamp reference designations shown in parentheses in the VERIFICATION column provide a troubleshooting aid for identifying the most probable cause of failure for that particular step in the test.***

6.05 ***Fuses:*** Failure of one or more fuses may be detected from indications at the front panel of the test set. To gain access to the fuses, remove the rear cover as explained in 6.03. The following procedure gives indications of ***open*** fuses. If the fuse has failed, the condition under PROCEDURE should be observed.

Fuse Test

STEP	PROCEDURE
	F1 BAD
1	Operate the POWER switch. The POWER lamp will remain extinguished and the set will be inoperative with the exception of the dc voltmeter.
	F2
2	Set the TEST MODE switch to RCV SER and the BIT RATE switch to EXT+. The NO DATA and NO CLOCK lamps remain extinguished. DISPLAY LITE BURNED

STEP	PROCEDURE
	F3
3	Set the FUNCTION switch to VOLT INT and the RANGE switch to DCV/10. Set the SELECT switch to +2.0 and the OUTPUT switch to TP3. Set the VERTICAL MONITOR switch to 1 and the POLARITY switch to NOR. At the matrix, insert a programming (shorting) pin in row TP3, column 1. The meter indicates 0 dc volts with the SELECT switch in any of the plus voltage positions. Remove the programming pin. DISPLAY LITE BLURRED
	F4
4	Set the FUNCTION switch to VOLT INT and the RANGE switch to DCV/10. Set the SELECT switch to -2.0 and the OUTPUT switch to TP3. Set the VERTICAL MONITOR switch to 1 and the POLARITY switch to ▶REV.◀ At the matrix, insert a programming (shorting) pin in row TP3, column 1. The meter indicates 0 dc volts with the SELECT switch in any of the minus voltage positions. Remove the programming pin.
	F5
5	Set FUNCTION switch to VOLT/OHM EXT. Set the RANGE switch to X1. Strap across INPUT terminals with test lead. Adjust ZERO OHMS control. The meter pointer will not zero and remains near midscale.

6.06 ***Reference Voltage:*** The reference voltage circuit is a precision supply and divider circuit that develops fixed selectable voltages of +7, ±2, ±1 and ±0.477 dc volts. In addition, a voltage adjustable over a 0 to +8 dc volt range is available. The following test permits checking these voltages with the 914B test set meter.

Reference Voltage

STEP	ACTION	VERIFICATION
1	At test set—	
	Insert a programming (shorting) pin in matrix, row TP3, column 1.	
2	Set OUTPUT switch to ▶OFF.◀	
3	Operate POWER switch.	POWER lamp lit.
4	Set FUNCTION switch to VOLT INT.	
5	Set RANGE switch to DCV/10.	
6	Set POLARITY switch to NOR.	
7	Set VERTICAL MONITOR switch to 1.	
8	Set both coarse (outer) and fine (inner) ADJUST controls fully counterclockwise.	

STEP	ACTION	VERIFICATION
9	Set SELECT switch to ADJ.	
10	Set OUTPUT switch to TP3.	Meter indicates 0 dc volts.
11	Rotate both coarse and fine ADJUST controls fully clockwise.	Meter pointer varies smoothly and indicates +10.0, ±0.5 dc volts with both controls fully clockwise.
12	Rotate fine (small) control fully counterclockwise.	Meter indicates at least 0.5 volt dc less than value read in Step 11.
13	Observing meter polarity— Rotate SELECT switch through succeeding positions as shown in Table F.	Meter indications as shown in Table F.

TABLE F

REFERENCE VOLTAGES

SET SELECT SWITCH TO:	SET RANGE DCV SWITCH TO:	METER INDICATES BETWEEN:	SET POLARITY SWITCH TO:
−2.0	3	−1.90 to −2.10	REV
−1.0	1	−0.95 to −1.05	REV
−.477	1	−0.45 to −0.5	REV
0	1	0	—
+.477	1	+0.45 to +0.5	NOR
+1.0	1	+0.95 to +1.05	NOR
+2.0	3	+1.90 to +2.10	NOR
+7.0	10	+6.65 to +7.35	NOR

14	Operate POWER switch.	POWER lamp extinguished.
15	Remove test connections.	

6.07 ***Control Signals:*** The control signal portion of the test set consists of DS1 through DS8 indicator lamps and S1 through S8 toggle switches. The INTERFACE MODE switch permits control with either contact closures or application of control voltages. It should be noted that the toggle switches are independent of the lamps. By properly programming the matrix, any lamp may be controlled by any switch. The following test verifies that the eight lamps may be operated by a contact closure or voltage as controlled by switches through programmed matrix connections.

Control Signals

STEP	ACTION	VERIFICATION
1	At test set— Insert shorting pin in matrix, row S1, column 1.	

STEP	ACTION	VERIFICATION
2	Insert shorting pin in matrix, row DS1, column 1.	
3	Set S1 through S8 toggle switches to OFF.	
4	Operate POWER switch.	POWER lamp lit.
5	Set INTERFACE MODE switch to CONTACT.	DS1 through DS8 lamps extinguished.
6	Set S1 toggle switch to ON.	DS1 lamp lit. (DS1 lamp).
7	Set S1 toggle switch to OFF.	DS1 lamp extinguished.
8	Test circuits for the switches and lamps as shown in Table G.	DS2 through DS8 lamps operate as shown in Table G. (DS2 through DS8 lamps, CP8). ***Note:*** If an indicator lamp fails to light with the INTERFACE MODE switch set to CONTACT, the corresponding position may

TABLE G

CONTROL SIGNALS

CONNECT MATRIX		OPERATE		OBSERVE	
ROW	COLUMN	SWITCH	POSITION	LAMP	INDICATION
DS2 S2	2 2	S2	ON OFF	DS2	Lit Extinguished
DS3 S3	3 3	S3	ON OFF	DS3	Lit Extinguished
DS4 S4	4 4	S4	ON OFF	DS4	Lit Extinguished
DS5 S5	5 5	S5	ON OFF	DS5	Lit Extinguished
DS6 S6	6 6	S6	ON OFF	DS6	Lit Extinguished
DS7 S7	7 7	S7	ON OFF	DS7	Lit Extinguished
DS8 S8	8 8	S8	ON OFF	DS8	Lit Extinguished

STEP	ACTION	VERIFICATION
		be tested with the voltmeter. Set the FUNCTION switch to VOLT INT, RANGE switch to DCV/30 and select the desired matrix connection using the VERTICAL MONITOR switch. The meter will indicate 0 volts for a lamp failure. If the meter indicates +23 dc volts, the trouble is internal to the 914B.
9	Set INTERFACE MODE switch to VOLTAGE.	DS1 through DS8 lamps extinguished.
10	Repeat Steps 6, 7 and 8.	Same as in Steps 6, 7, 8 and Table G. (DS1 through DS8 lamps, CP8). ***Note:*** If an indicator lamp fails to light with the INTERFACE MODE switch set to VOLTAGE, the corresponding position may be tested with the voltmeter. Set the FUNCTION switch to VOLT INT, RANGE switch to DCV/10, and select the desired matrix connection using the VERTICAL MONITOR switch. A meter indication of +4.0 $\pm$0.3 dc volts should be observed for toggle switches that are ON and −4.0 $\pm$0.3 dc volts for switches that are OFF.
11	Operate POWER switch.	POWER lamp extinguished.
12	Remove test connections.	

6.08 ***Interval Counter:*** The 914B provides an interval counter which may be used to detect the first occurrence of a preselected signal transition, measure time between pulses or measure pulse length. The following test checks the first occurrence feature and provides a test of the counter display.

STEP	ACTION	VERIFICATION
Interval Counter		
1	At test set— Set S1 through S8 toggle switches to OFF.	
2	Insert shorting pin in matrix, row TP1, column 1.	
3	Insert shorting pin in matrix, row S1, column 1.	
4	Insert shorting pin in matrix, row TP2, column 2.	
5	Insert shorting pin in matrix, row S2, column 2.	

STEP	ACTION	VERIFICATION
6	Operate FUNCTION switch to OFF.	
7	Operate POWER switch.	POWER lamp lit.
8	Set INTERFACE MODE switch to CONTACT.	
9	Set BIT RATE switch to 2400.	
10	Set TEST MODE switch to TRMT SER.	
11	Set TRIGGER TP1 and TRIGGER TP2 switches to −/CLOSE.	
12	Set COUNTER switch to INTERVAL/X100.	
13	Momentarily operate RESET switch.	Counter display reads 00.
14	Using a suitable timer— Set ◗S1◖ toggle switch to ON.	Counter display starts.
15	After 5 seconds— Set ◗S2◖ toggle switch to ON.	Counter display stopped at approximately 50. FIRST TP1 lamp lit. (FIRST TP1 lamp).
16	Set TRIGGER TP1 and TRIGGER TP2 switches to +/OPEN.	
17	Momentarily operate RESET switch.	Counter display reads 00.
18	Using a suitable timer— Set S2 toggle switch to OFF.	Counter display starts.
19	After 5 seconds— Set S1 toggle switch to OFF.	Counter display stopped at approximately 50. FIRST TP2 lamp lit. (FIRST TP2 lamp).
20	Operate POWER switch.	POWER lamp extinguished.
21	Remove shorting pins from matrix.	

6.09 ***Word Generator and Clock:*** The 914B word generator will produce three different test messages: a dot signal, a 63-bit test message and a 511-bit test message. The bit rate of these signals may be determined by the test set clock, which may be varied in steps from 150 to 2400 bps. The following procedure determines that the test set will generate the required test signals and that the clock rate is variable.

STEP	ACTION	VERIFICATION
	Word Generator and Clock Circuits	
1	At test set— Set controls and establish connections as shown in Fig. 16.	
2	Operate POWER switch.	POWER indicator lamp lit.
3	Set RANGE switch to 1 VAC.	
4	Set FUNCTION switch to VOLT OHM/EXT.	NO DATA lamp extinguished. NO CLOCK lamp extinguished. (CP1, CP2, CP4). Meter indicates .60 $\pm$.50 volt ac. (CP3, CP4).
5	Set WORD LENGTH switch to 511.	Meter indicates .60 $\pm$.05 volt ac. (CP3).
6	Set WORD LENGTH switch to DOT.	Meter indicates ◗.75 $\pm$.075◖ volt ac. (CP3).
7	Set FUNCTION switch to OFF.	
8	Set BIT RATE switch to 150.	
9	Set WORD LENGTH switch to 63.	
10	Set TEST SET MODE switch to RCV SER.	Counter display indicates counting. NO DATA lamp lights after brief pause. (NO DATA lamp, CP4).
11	Operate and hold RESET switch.	Counter display reads 00. (CP1). OVERFLOW lamp remains extinguished.
12	Release RESET switch.	Counter display will count. OVERFLOW lamp lights when count goes from 99 to 00. (OVERFLOW lamp).
13	Rotate BIT RATE switch through all 150 through 2400 positions.	Counter display rate increases for each increasing BIT RATE switch position. (CP1, CP2).
14	Set BIT RATE switch to EXT+.	Counter display stopped. NO CLOCK lamp lit after brief pause. (NO CLOCK lamp, CP4).
15	Set BIT RATE switch to EXT−.	Counter display remains stopped. NO CLOCK lamp remains lit.
16	Set FUNCTION switch to VOLT OHM/EXT.	
17	Set TEST SET MODE switch to TRMT SER.	NO CLOCK lamp ◗lit.◖ NO DATA lamp ◗lit.◖

STEP	ACTION	VERIFICATION
18	Set RANGE switch to 1/DCV.	Meter indicates 0.7 ±0.1 dc volt. ***Note:*** If meter reads downscale set POLARITY switch to opposite position. (CP4).
19	Operate BIT RATE switch between EXT+ and EXT− until proper meter indication is obtained.	Meter reads downscale.
20	Set POLARITY switch to opposite position.	Meter indicates 0.7 ±0.1 dc volt. (CP4).
21	Set RANGE switch to 10/DCV.	
22	Set SIGNAL LEVEL switch to ±4V.	
23	Repeat Steps ➧19 and 20➧.	Meter indicates 4.0 ±0.5 dc volts. (CP4).
24	Set FUNCTION switch to OFF.	
25	Set SIGNAL LEVEL switch to ±.7V.	
26	Set BIT RATE switch to 1600.	
27	Set RANGE switch to 1/ACV.	
28	Set FUNCTION switch to SPKR.	Raspy noise heard in loudspeaker.
29	Rotate RANGE switch through all ACV positions.	Loudspeaker level increases as switch is rotated ccw.
30	Operate POWER switch.	POWER lamp extinguished.
31	Remove test connections.	

6.10 ***Parallel Data Circuits:*** The 914B develops an output signal for testing Data Sets 402-type. The signal represents either an open or closed contact. The following procedure checks that the test set will generate either a dotting signal or a random test message and that the signal will appear on the proper leads.

STEP	ACTION	VERIFICATION
Parallel Data Circuits		
1	At test set— Set controls and establish test connections as shown in Fig. 17.	
2	Operate POWER switch.	POWER indicator lamp lit.
3	Set FUNCTION switch to VOLT/OHM EXT.	
4	Insert shorting pin in matrix, row TP1, column 2.	Meter indicates ➧0.7 to 0.9➧ volt ac. (CP5, CP8).

STEP	ACTION	VERIFICATION
5	Repeat Step 4 for columns 3, 4, 5 and 7, 8, 9, 10.	Same as Step 4.
6	Insert shorting pin in matrix, row TP1, column 6.	Meter indicates ▶0.5 to 0.6◀ volt ac. (CP5, CP8).
7	Set WORD LENGTH switch to 63.	
8	Set TEST MODE switch to ALL RANDOM.	
9	Remove shorting pin from matrix, row TP1, column 6.	
10	Repeat Steps 4 and 5.	Meter indicates ▶0.4 to 0.7◀ volt ac. (CP5, CP8). ***Note:*** Meter pointer "jitters" as result of random test message.
11	Set TEST MODE switch to CHAN/1.	
12	Insert shorting pin in matrix, row TP1, column 2.	Meter indicates ▶0.35 to 0.55◀ volt ac.
13	Set TEST MODE switch to CHAN/2.	
14	Insert shorting pin in matrix, row TP1, column 3.	Meter indicates ▶0.35 to 0.55◀ volt ac.
15	Set TEST MODE switch to CHAN/3.	
16	Insert shorting pin in matrix, row TP1, column 4.	Meter indicates ▶0.35 to 0.55◀ volt ac.
17	Set TEST MODE switch to CHAN/4.	
18	Insert shorting pin in matrix, row TP1, column 5.	Meter indicates ▶0.35 to 0.55◀ volt ac.
19	Set TEST MODE switch to CHAN/5.	
20	Insert shorting pin in matrix, row TP1, column 7.	Meter indicates ▶0.35 to 0.55◀ volt ac.
21	Set TEST MODE switch to CHAN/6.	
22	Insert shorting pin in matrix, row TP1, column 8.	Meter indicates ▶0.35 to 0.55◀ volt ac.
23	Set TEST MODE switch to CHAN/7.	
24	Insert shorting pin in matrix, row TP1, column 9.	Meter indicates ▶0.35 to 0.55◀ volt ac.

STEP	ACTION	VERIFICATION
25	Set TEST MODE switch to CHAN/8.	
26	Insert shorting pin in matrix, row TP1, column 10.	Meter indicates ▶0.35 to 0.55◀ volt ac.
27	Operate POWER switch.	POWER lamp extinguished.
28	Remove all test connections.	

6.11 ***Word Generator, Clock and Sync Circuits:*** This test utilizes two 914B Data Test Sets and checks the data and clock circuits of one set when used as a transmitter, and the second test set when used as a receiver. To facilitate testing, these circuits are tested as a group, rather than individually.

STEP	ACTION	VERIFICATION
	Word Generator, Clock and Sync Circuits	
1	At test sets A and B— Set controls and establish test connections as shown in Fig. 18.	
2	Operate POWER switches.	POWER indicator lamps lit.
3	At test set A— Insert shorting pin in matrix, row SD, column 2.	At test set B— Meter pointer deflects. (CP1, CP2, CP3, CP4).
4	Adjust PHASE control of test set B for meter indication.	Meter pointer nulls to 0. (CP1, CP2, CP3, CP4).
5	Set FUNCTION of test set B switch to OFF.	NO DATA and NO CLOCK lamps are extinguished. Counter display starts. (CP3, CP4).
6	Momentarily operate WORD SYNC of test set B switch to MAN.	Counter display stops.
7	At test set A— Operate WORD LENGTH switch to 511 then return to 63.	At test set B— Counter display starts.
8	Set WORD SYNC switch to AUTO.	Counter display stops.
9	At test sets A and B— Set WORD LENGTH switches to 511.	At test set B— Counter display may run momentarily then stop. (CP3).
10	At test sets A and B— Set BIT RATE switches to 300.	
11	At test set B— Set FUNCTION switch to PHASE ADJ.	

STEP	ACTION	VERIFICATION
12	Adjust PHASE control for zero indication.	Meter pointer indicates 0.
13	Set FUNCTION switch to OFF.	Counter display may run momentarily, then stop. (CP1).
14	Repeat Steps 10 through 13 for each BIT RATE switch position through 2400.	Same as Steps 10 through 13.
15	At test set B— Set WORD SYNC switch to OFF.	
16	At test set A— Set WORD LENGTH switch to 63.	
17	At test set B— Set COUNTER switch to BLOCK ERRORS/WL.	Counter display runs at slower rate. (CP5, CP8).
18	Advance COUNTER switch through each BLOCK ERROR position through 16 WL.	Counter display runs at decreasing rate for each increasing word length position. (CP5, CP8).
19	At test sets A and B— Operate POWER switches.	POWER lamps extinguished.
20	Remove all test connections.	
	Note: To test the respective transmitting and receiving functions of test sets A and B, exchange the sets serving as transmitter and receiver and repeat the test procedure.	

6.12 ***Parallel Data Circuits:*** This test provides a check of both the transmitting and receiving capabilities of two 914Bs conditioned for testing Data Sets 402-type.

STEP	ACTION	VERIFICATION
	Parallel Data Circuits	
1	At test sets A and B— Set controls and establish test connections as shown in Fig. 19.	
2	Operate POWER switches.	POWER lamps lit. At test set B— Counter display runs.
3	Momentarily operate WORD SYNC switch to MAN.	Counter display stops.
4	At test sets A and B— Set TEST MODE switches to CHAN 1.	At test set B— Counter display runs.

STEP	ACTION	VERIFICATION
5	Momentarily operate WORD SYNC switch to MAN.	Counter display stops.
6	Repeat Steps 4 and 5 for each TEST MODE/CHAN postion 2 through 8.	Same as Steps 4 and 5.
7	At test sets A and B— Operate POWER switches.	POWER lamps extinguished.
8	Remove all test connections. ***Note:*** To test the respective transmitting and receiving functions of test sets A and B, exchange the sets serving as transmitter and receiver and repeat the test procedure.	

6.13 ***Clock Circuits:*** The following test uses an electronic counter to provide a readout of the internal test set clock. A test of the 75-Hz parallel data clock is also provided.

STEP	ACTION	VERIFICATION
	Clock Circuits	
1	At test set and counter— Set controls and establish test connections as shown in Fig. 20.	
2	Operate POWER switches.	POWER lamp lit and counter energized. ***Note:*** Allow test set and counter a 5-minute warm-up period before proceeding with test.
3	Set BIT RATE switch to each 150 through 2400 postion and observe counter readings as shown in BIT RATE AND CLOCK chart on test diagram.	Counter reads within tolerances for each setting of BIT RATE switch. (CP1, CP2).
4	Set COUNTER switch to each INTERVAL/X.1 through X100 position and observe counter readings as shown in BIT RATE TEST table on Fig. 20.	Counter reads within tolerances for each setting of COUNTER switch. (CP1, CP2).
5	At test set— Set BIT RATE switch to EXT+.	
6	Set COUNTER switch to BIT ERRORS.	
7	Set TEST MODE switch to TRMT-402.	At counter— Counter reads 75 $\pm$4 Hz. (CP5).
8	At test set and counter— Operate POWER switches.	POWER lamp extinguished and counter de-energized.

6.14 ***Data and Sample Circuits:*** This test uses a dual trace oscilloscope equipped for external sync and a variable time base to monitor the data, sync and clock outputs. Nominal pulse deviation and amplitudes are given on the test connection diagram. The dual trace feature permits checking the phase relationship of the data and clock signals.

STEP	ACTION	VERIFICATION
	Data and Sample Circuits	
1	At test set and oscilloscope— Set controls and establish test connections as shown in Fig. 21.	
2	Operate POWER switches.	POWER lamp lit and oscilloscope energized.
3	At oscilloscope— Set controls to observe channel 2 input.	Observe waveform A on test diagram. (CP5, CP4).
4	Set controls to observe channel 1 input.	Observe waveform B on test diagram.
5	At test set— Set WORD LENGTH switch to 511.	
6	At oscilloscope— Set controls to observe channel 1 and 2 inputs.	Waveforms observed in Steps 3 and 4 do not change. (CP3).
7	Remove test lead connection between oscilloscope sync connector and channel 2 input, ◗leaving SYNC of test set connected to sync of oscilloscope.◖	
8	At test set— Connect test lead from oscilloscope channel 2 input to DATA OUT jack.	
9	At oscilloscope— Using external sync— Set controls to observe channel 1 and 2 inputs.	Observe waveform C shown on test diagram.
10	At test set— Set WORD LENGTH switch to 63.	At oscilloscope— Observe waveform D shown on test diagram. (CP3).
11	At test set— Set WORD LENGTH switch to DOT.	At oscilloscope— Using internal sync— Observe waveform E shown on test diagram. (CP3).
12	At test set— Remove oscilloscope test lead (channel 1 input) from CLOCK jack and connect to CP2, TP1 (see Fig. 15 for circuit pack location).	
13	Remove oscilloscope sync lead (sync input) from SYNC jack and connect to CLOCK jack.	

STEP	ACTION	VERIFICATION
14	At oscilloscope— Set controls to adjust time base so that one bit interval of the data signal occupies a 10 CM sweep on the graticule.	Observe waveform F shown on test diagram. (CP3).
15	At test set— Operate SAMPLE WIDTH switch through each 10-50% positive.	At oscilloscope— The pulse width of channel 1 input shall be within $\pm$4% of the value for each switch position. Each pulse is centered within 2% along the vertical axis of the oscilloscope. (CP1, CP2).
16	At test set and oscilloscope— Operate POWER switches.	POWER lamp extinguished and oscilloscope de-energized.
17	Remove test connections.	

6.15 ***A. C. Voltmeter:*** The ac voltmeter portion of the meter circuit facilitates the measurement of voice-frequency signals in five 10-dB ranges (from 10 millivolts to 1 volt full-scale). The following test provides a method of calibrating the meter with a known ac reference voltage. Since the type of signal generator will vary at different telephone company locations, the test procedure is of a general nature.

STEP	PROCEDURE
1	Energize a reference generator (a 71-type milliwatt generator is suitable) having a known output.
2	Energize the 914B test set and set the FUNCTION switch to VOLT/OHM EXT.
3	Connect the reference generator output to the 914B INPUT terminals and read the applied signal on the lowest ac meter scale which will permit the nearest full-scale indication.
4	If the indication is not the same as the known reference, remove the rear cover as explained in 6.03 and adjust R17 (Fig. ▶15◀) until the meter indicates the same value as the applied signal.
5	Remove test connections and restore test equipment to normal operating conditions.

7. REFERENCES

7.01 Additional information on the 914B may be obtained from the following sources:

(a) SD- and CD-73056-01

(b) EL 278

(c) J-79914B-1

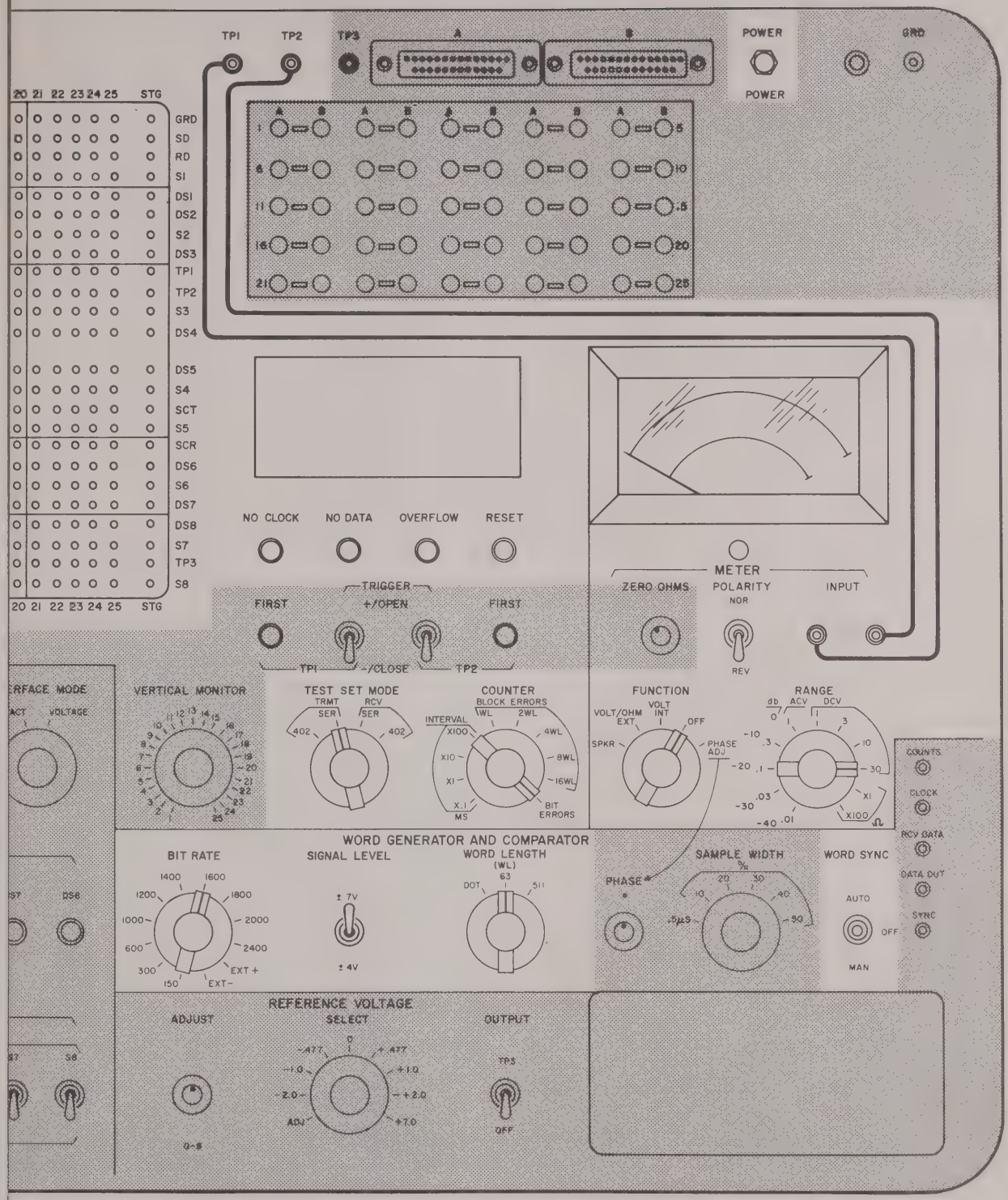

Fig. 16—Word Generator and Clock Circuits—Test Connections

STEP	ACTION	VERIFICATION
14	At oscilloscope— Set controls to adjust time base so that one bit interval of the data signal occupies a 10 CM sweep on the graticule.	Observe waveform F shown on test diagram. (CP3).
15	At test set— Operate SAMPLE WIDTH switch through each 10-50% positive.	At oscilloscope— The pulse width of channel 1 input shall be within $\pm$4% of the value for each switch position. Each pulse is centered within 2% along the vertical axis of the oscilloscope. (CP1, CP2).
16	At test set and oscilloscope— Operate POWER switches.	POWER lamp extinguished and oscilloscope de-energized.
17	Remove test connections.	

6.15 ***A. C. Voltmeter:*** The ac voltmeter portion of the meter circuit facilitates the measurement of voice-frequency signals in five 10-dB ranges (from 10 millivolts to 1 volt full-scale). The following test provides a method of calibrating the meter with a known ac reference voltage. Since the type of signal generator will vary at different telephone company locations, the test procedure is of a general nature.

STEP	PROCEDURE
1	Energize a reference generator (a 71-type milliwatt generator is suitable) having a known output.
2	Energize the 914B test set and set the FUNCTION switch to VOLT/OHM EXT.
3	Connect the reference generator output to the 914B INPUT terminals and read the applied signal on the lowest ac meter scale which will permit the nearest full-scale indication.
4	If the indication is not the same as the known reference, remove the rear cover as explained in 6.03 and adjust R17 (Fig. ▶15◀) until the meter indicates the same value as the applied signal.
5	Remove test connections and restore test equipment to normal operating conditions.

7. REFERENCES

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(b) EL 278

(c) J-79914B-1

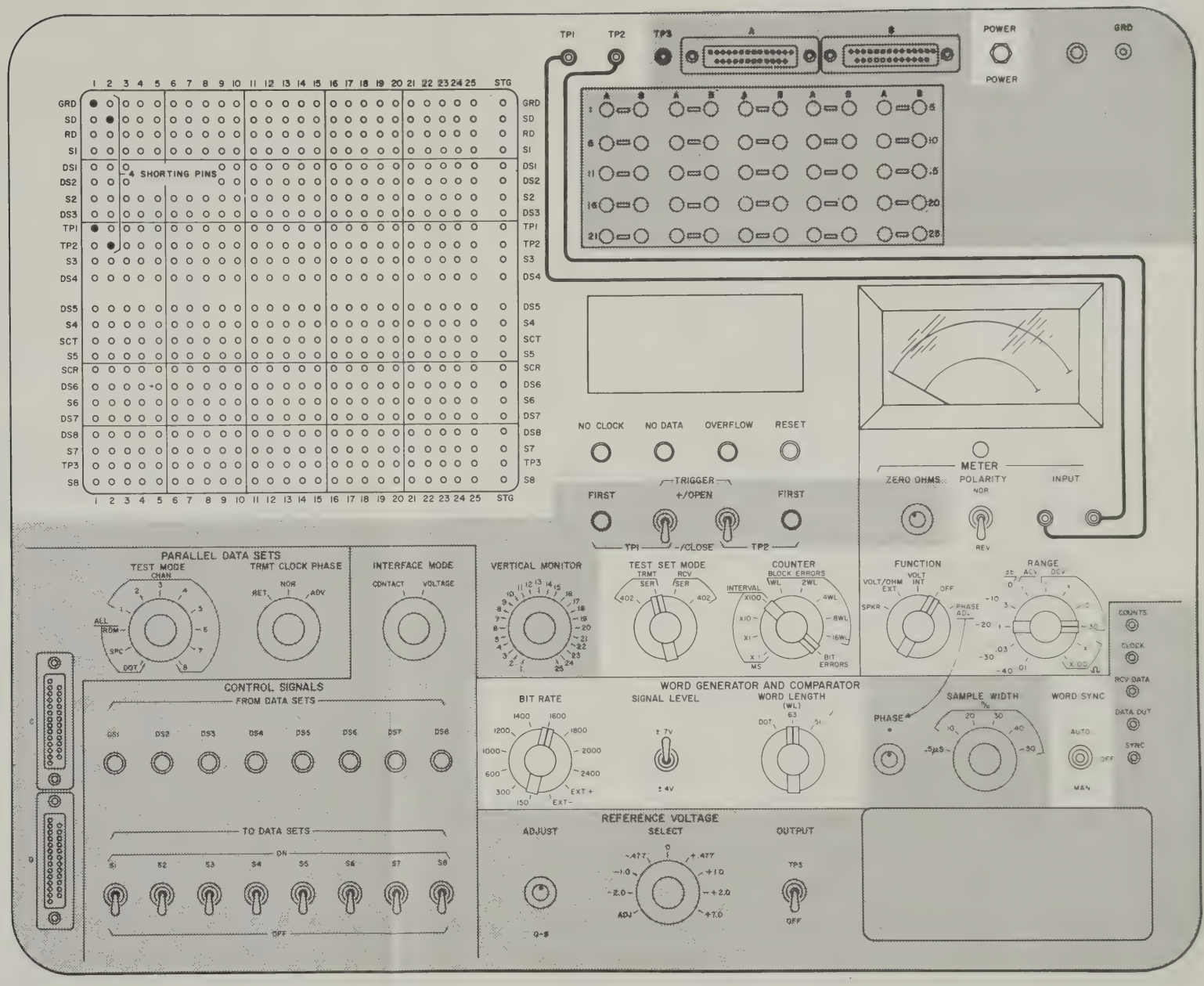


Fig. 16—Word Generator and Clock Circuits—Test Connections

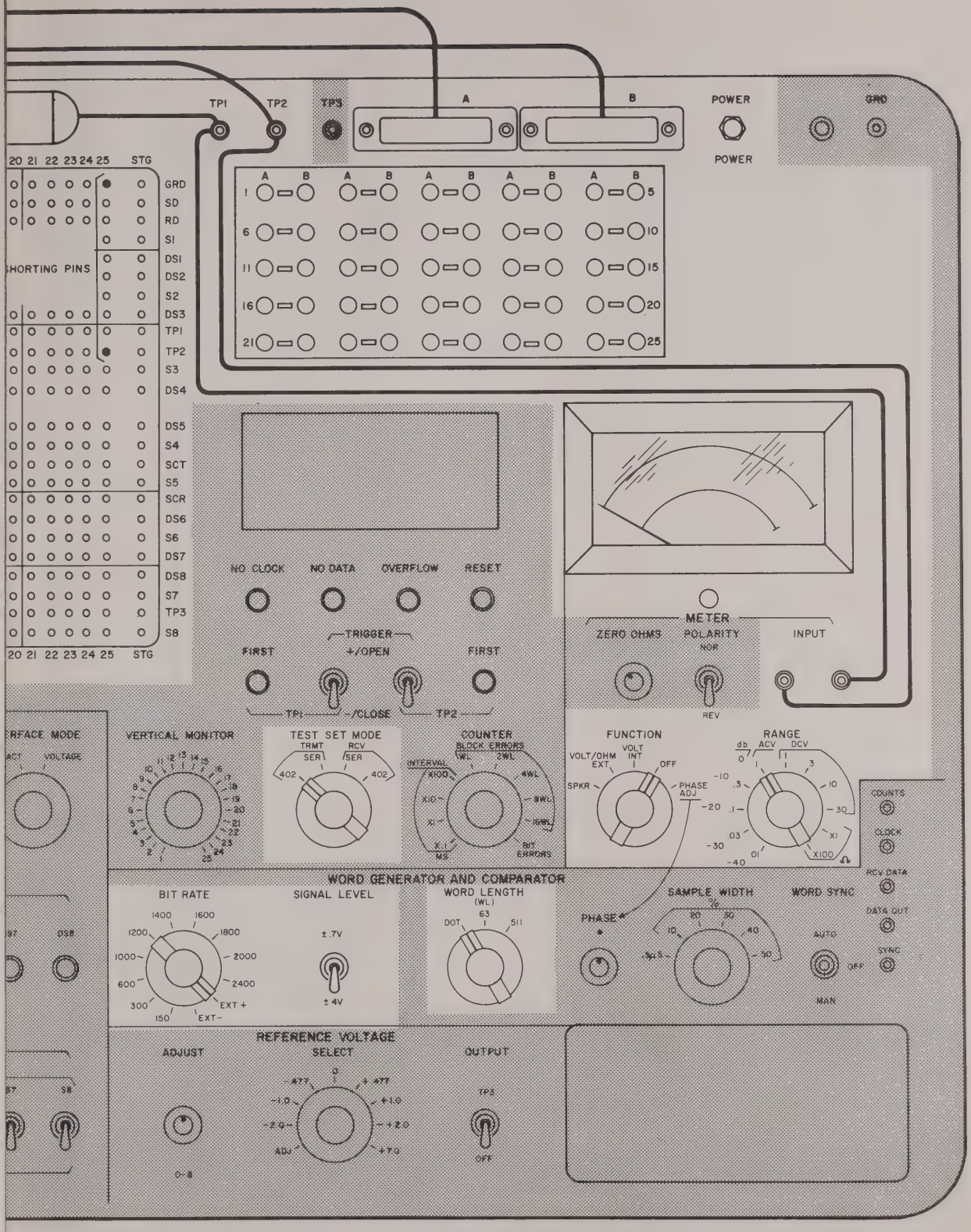


Fig. 17—Parallel Data Circuits—Test Connections

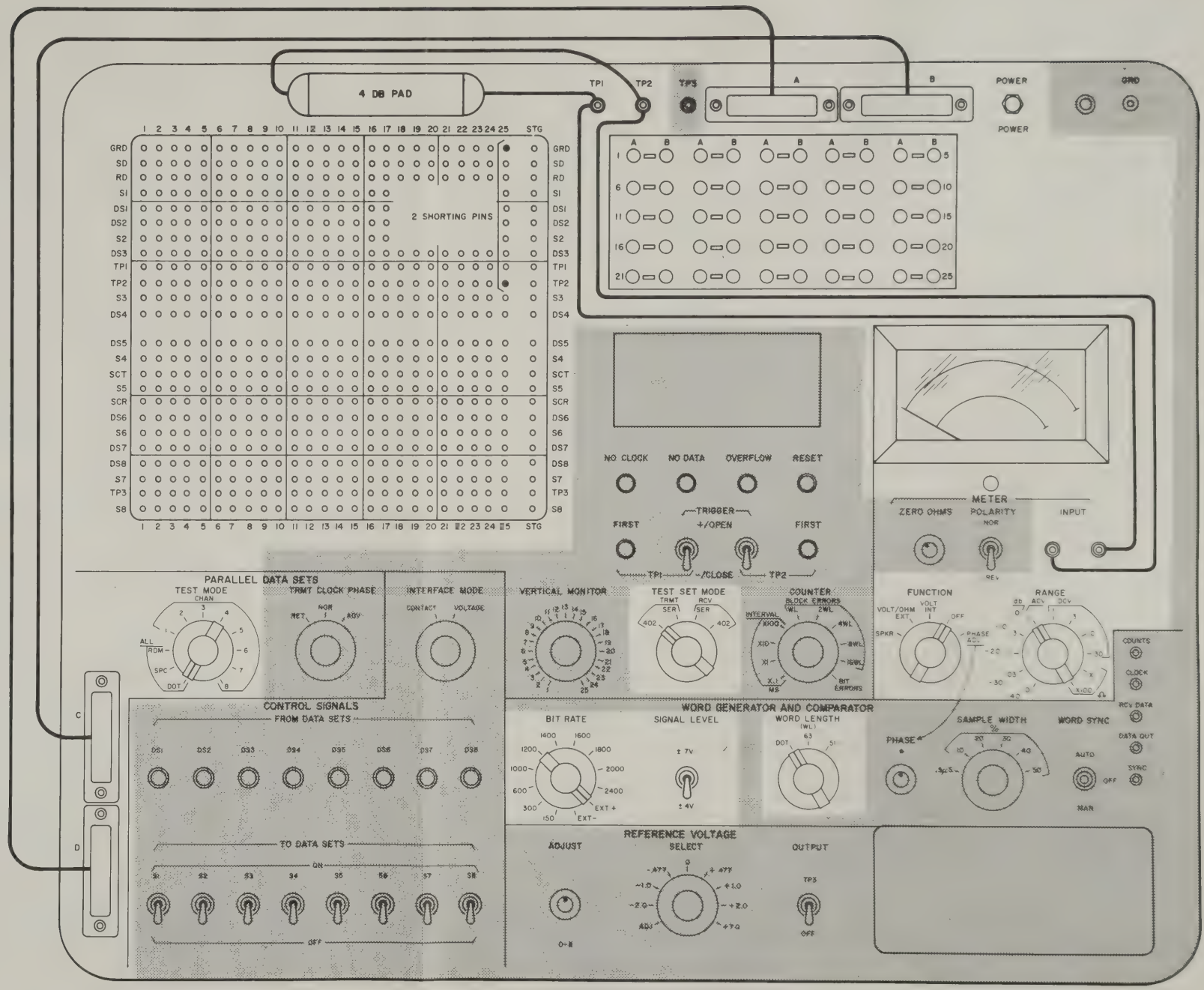
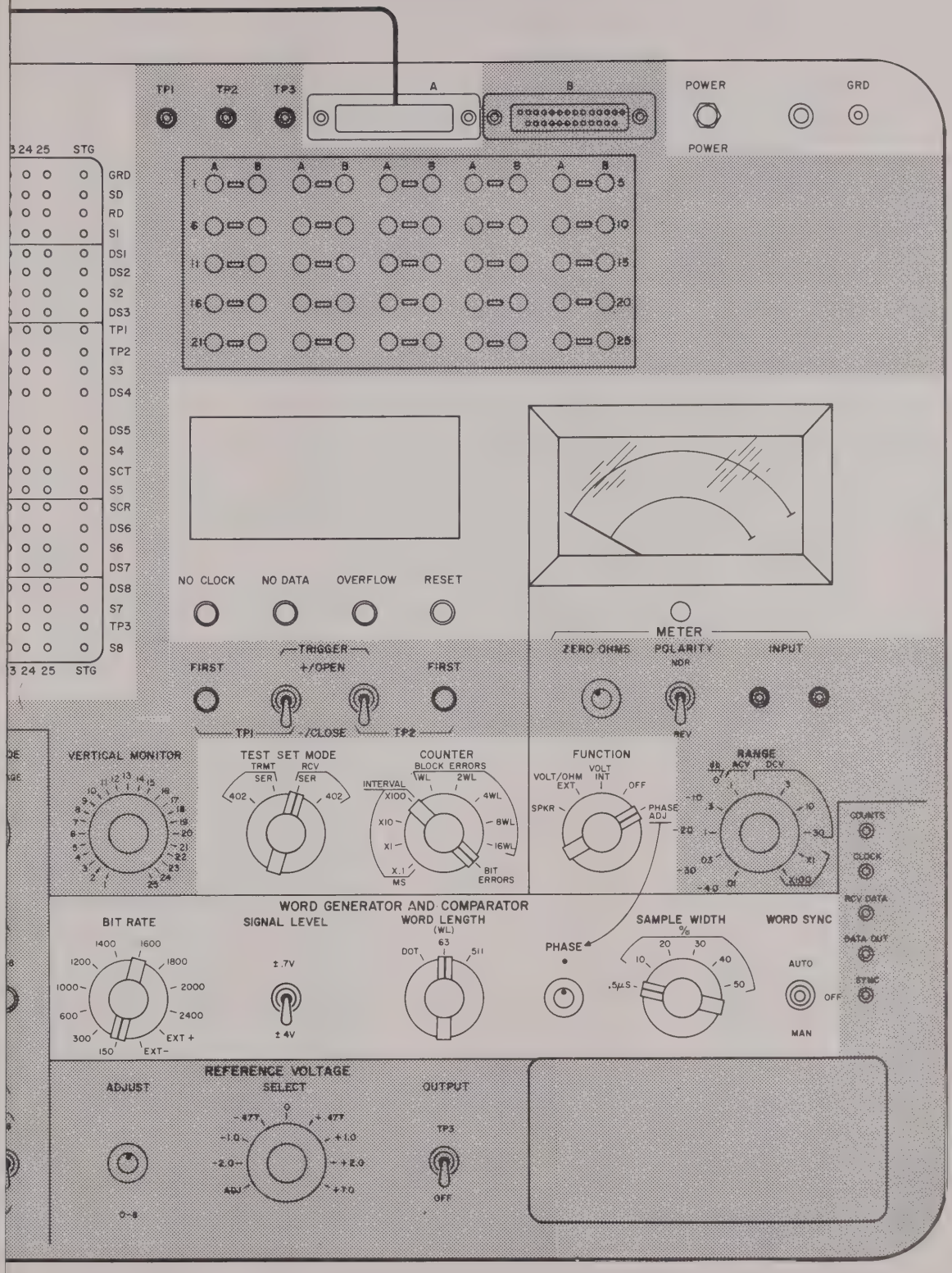


Fig. 17—Parallel Data Circuits—Test Connections



RECEIVING TEST SET – B

Fig. 18—Word Generator, Clock and Sync Circuits—Test Connections

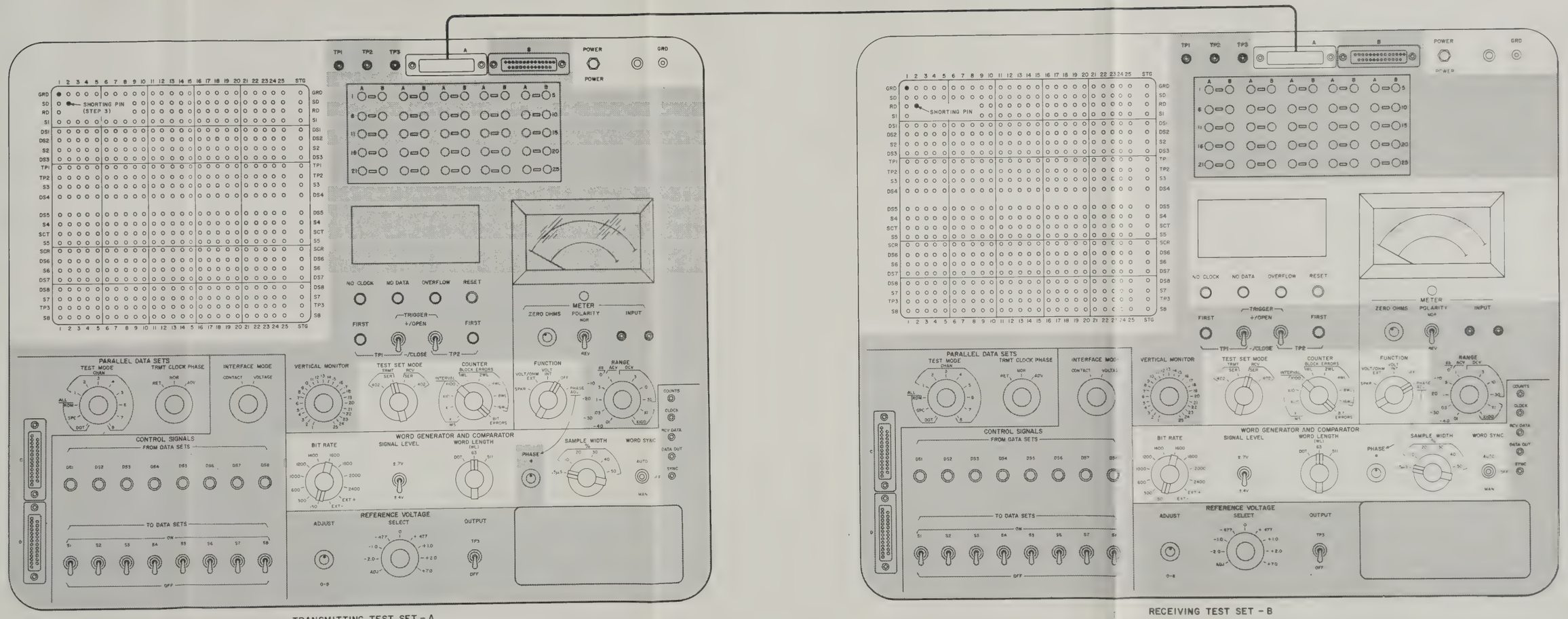
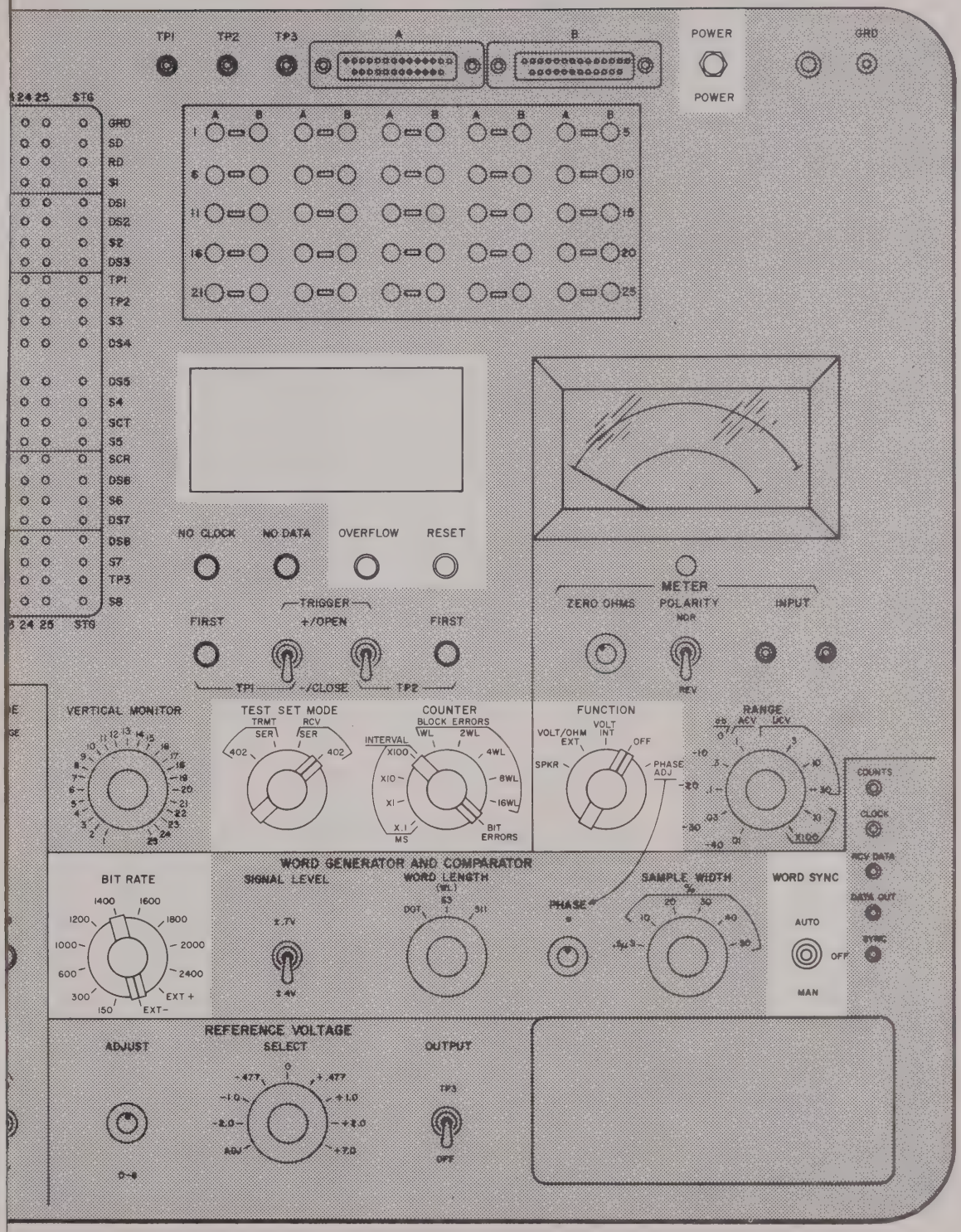
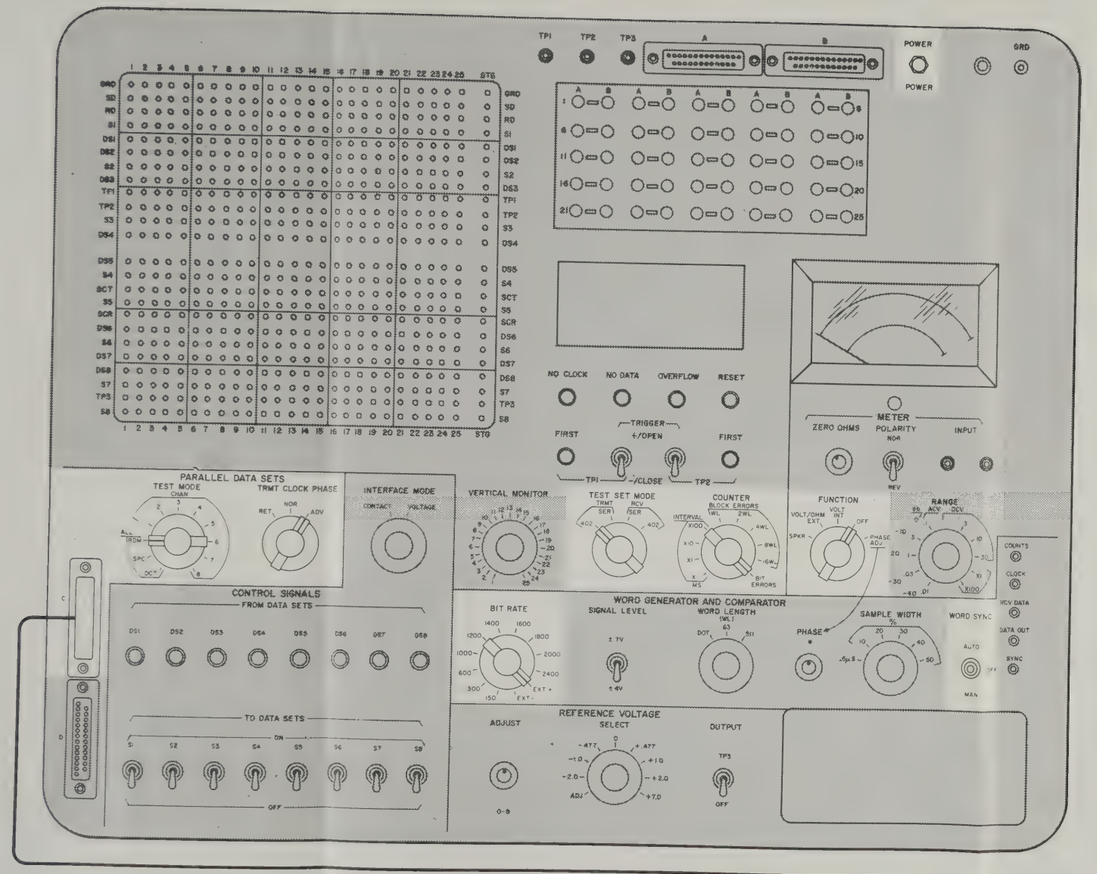


Fig. 18—Word Generator, Clock and Sync Circuits—Test Connections

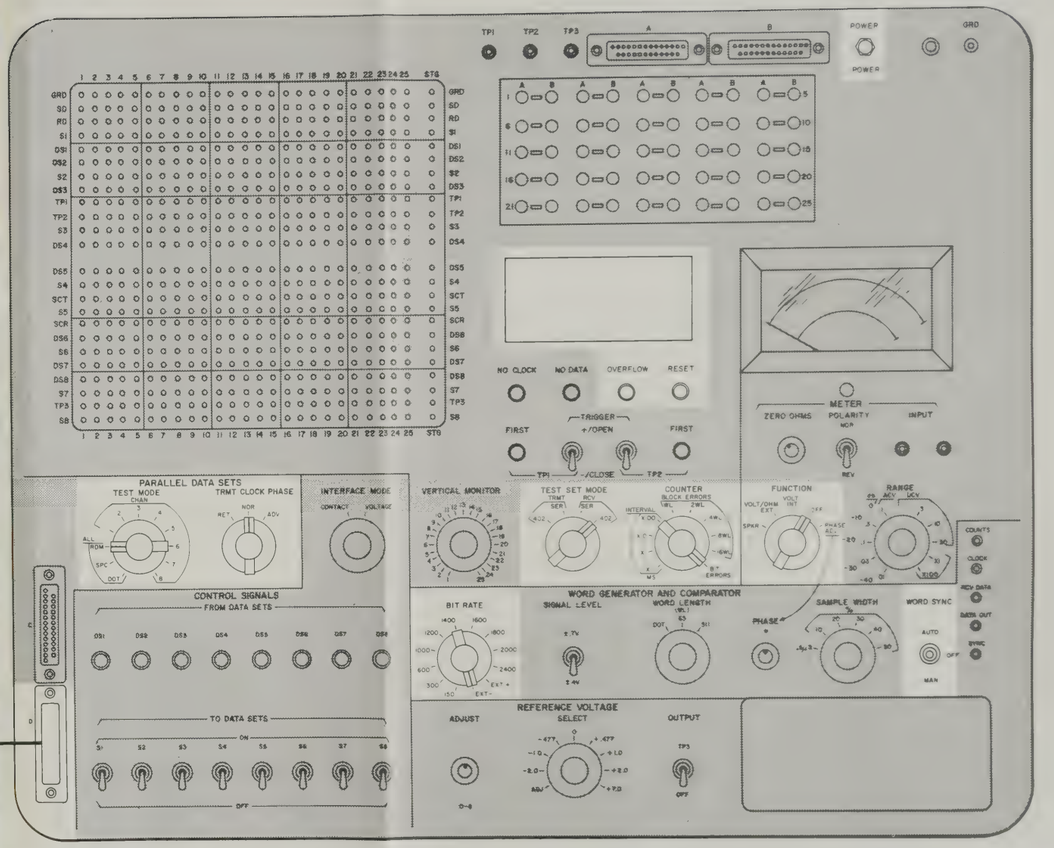


RECEIVING TEST SET - B

Fig. 19—Parallel Data Transmit and Receive Circuits—Test Connections



TRANSMITTING TEST SET – A



RECEIVING TEST SET – B

Fig. 19—Parallel Data Transmit and Receive Circuits—Test Connections

BIT RATE TEST

BIT RATE SWITCH POSITION	ELECTRONIC COUNTER FREQUENCY IN HZ
150	150 ± 5
300	300 ± 9
600	600 ± 18
1,000	1,000 ± 30
1,200	1,200 ± 36
1,400	1,400 ± 42
1,600	1,600 ± 48
1,800	1,800 ± 54
2,000	2,000 ± 60
2,400	2,400 ± 72
COUNTER SWITCH POSITION	
X .1	10,000 ± 250
X 1	1,000 ± 25
X 10	100 ± 3.0
X 100	10 ± 0.3

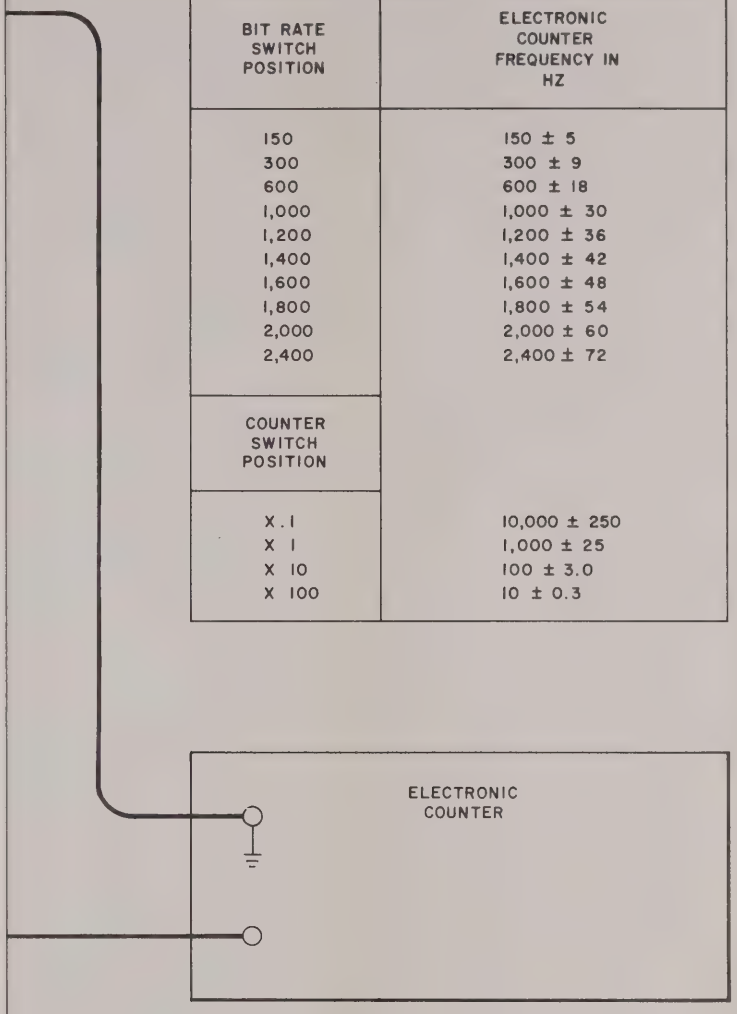
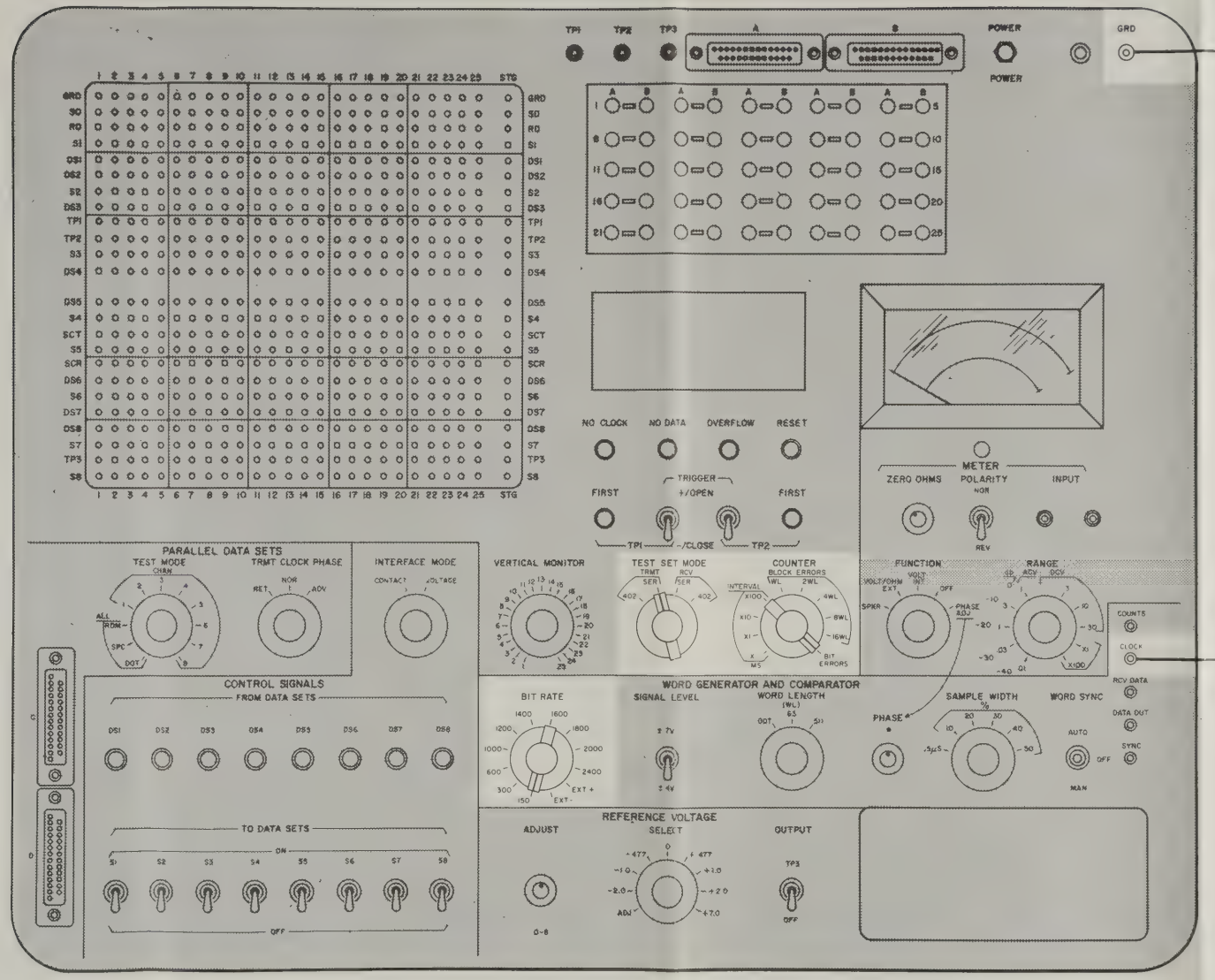


Fig. 20—Clock Circuit—Test Connections

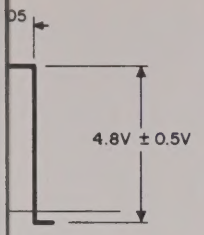


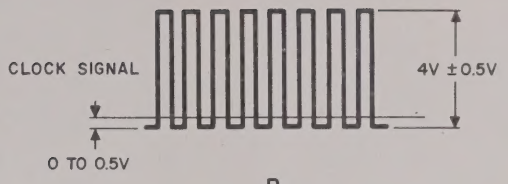
BIT RATE TEST

BIT RATE SWITCH POSITION	ELECTRONIC COUNTER FREQUENCY IN HZ
150	150 ± 5
300	300 ± 9
600	600 ± 18
1,000	1,000 ± 30
1,200	1,200 ± 36
1,400	1,400 ± 42
1,600	1,600 ± 48
1,800	1,800 ± 54
2,000	2,000 ± 60
2,400	2,400 ± 72
COUNTER SWITCH POSITION	
X .1	10,000 ± 250
X 1	1,000 ± 25
X 10	100 ± 3.0
X 100	10 ± 0.3

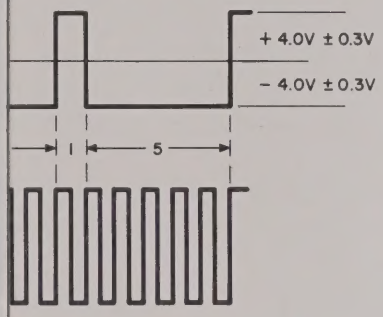
ELECTRONIC COUNTER

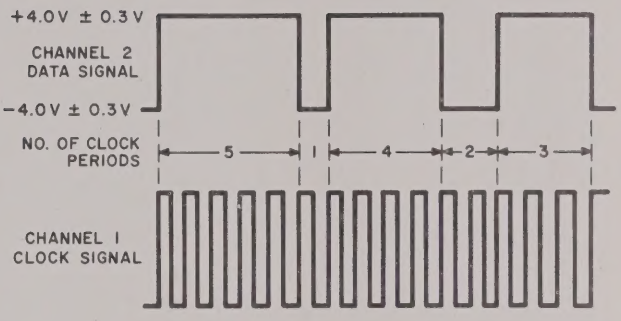
Fig. 20—Clock Circuit—Test Connections



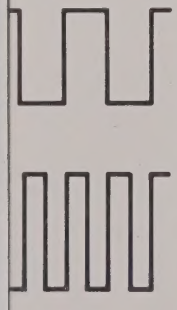


B

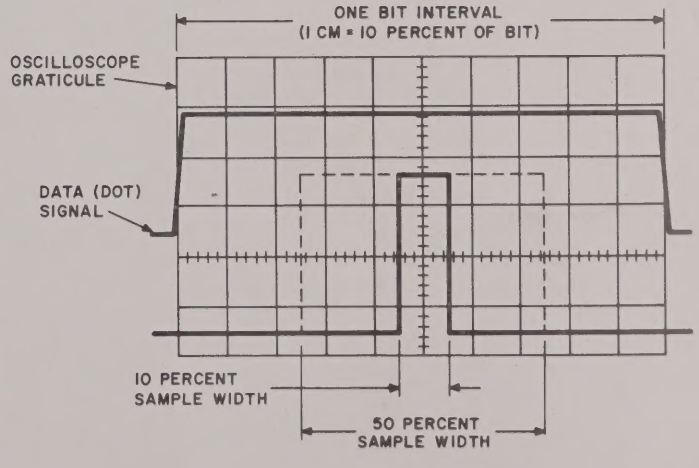




D

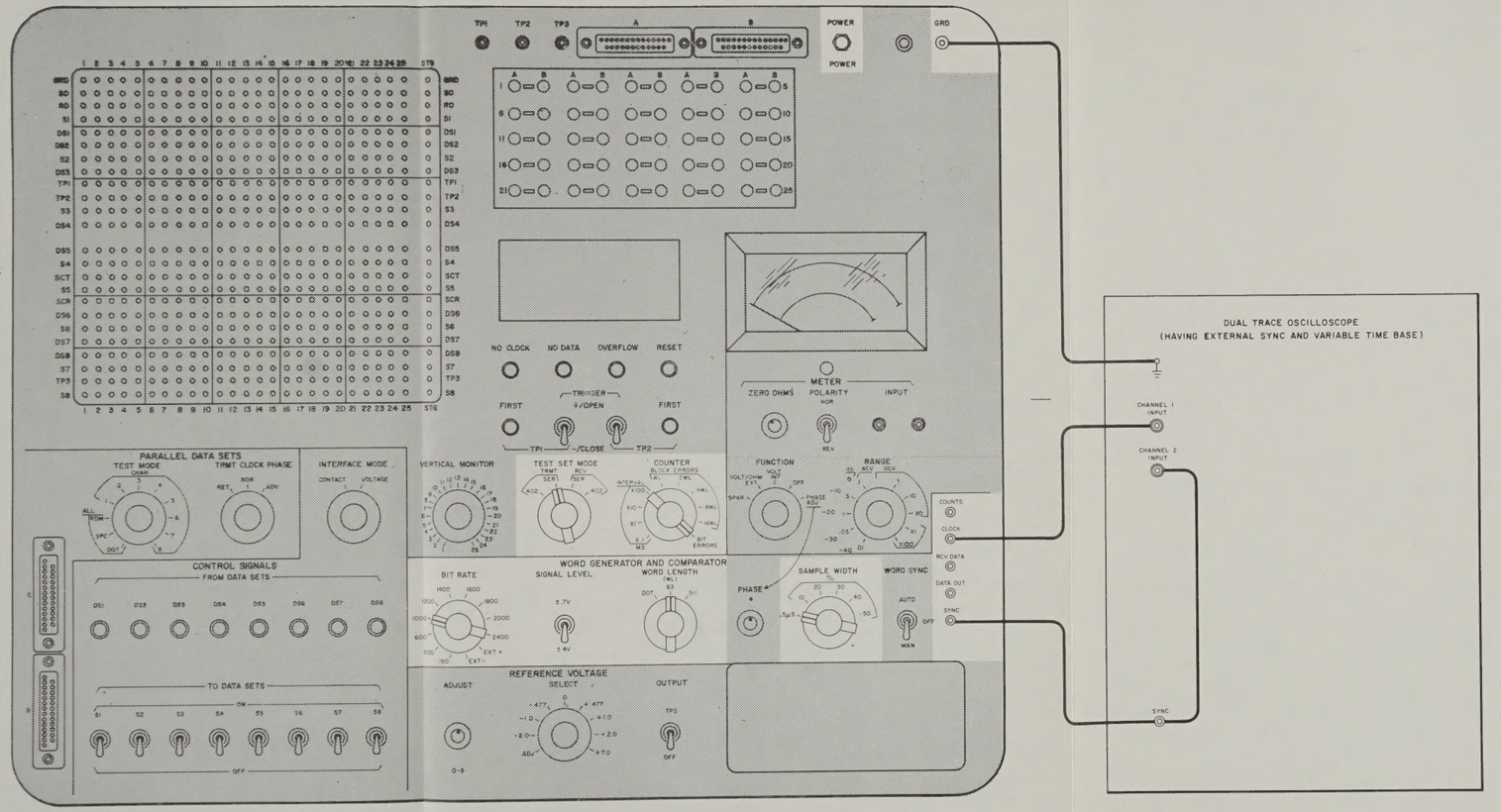


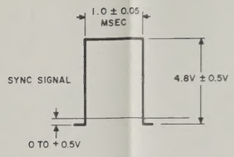
E

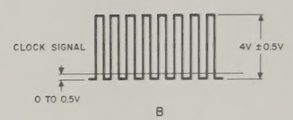


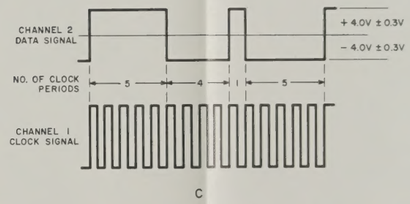
F

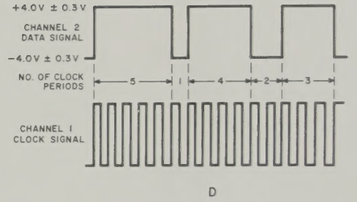
Fig. 21—Data and Sample Circuits—Test Connections

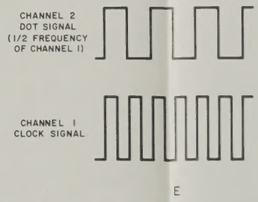












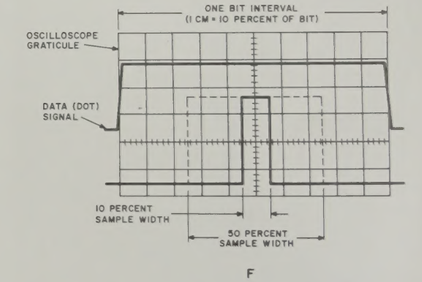


Fig. 21—Data and Sample Circuits—Test Connections